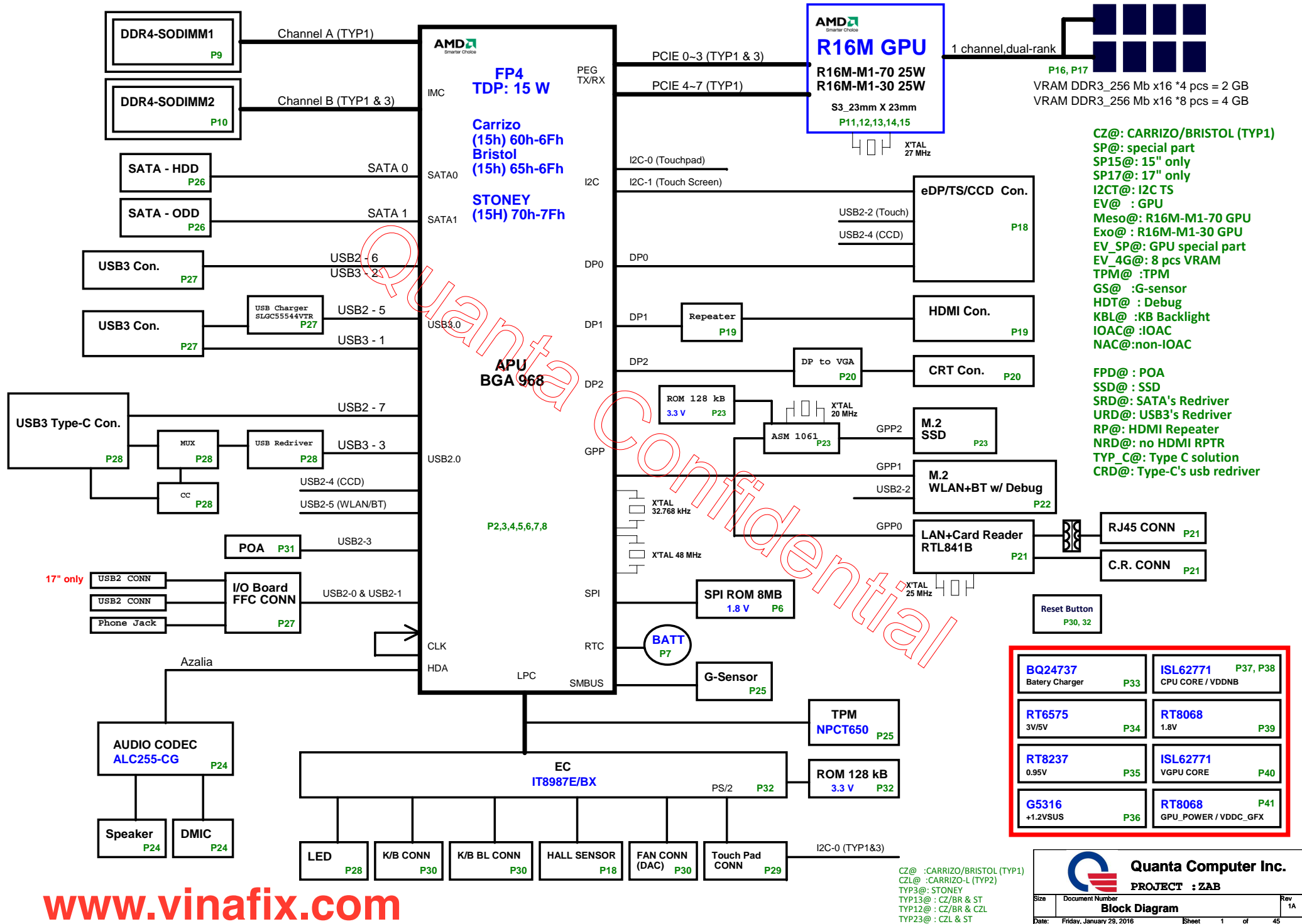
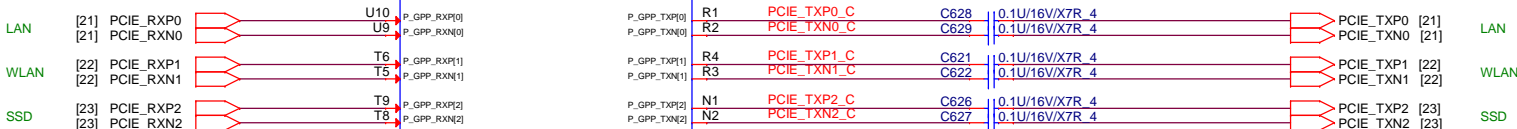


ZAB/ZAB A,B/ZYJA BLOCK DIAGRAM

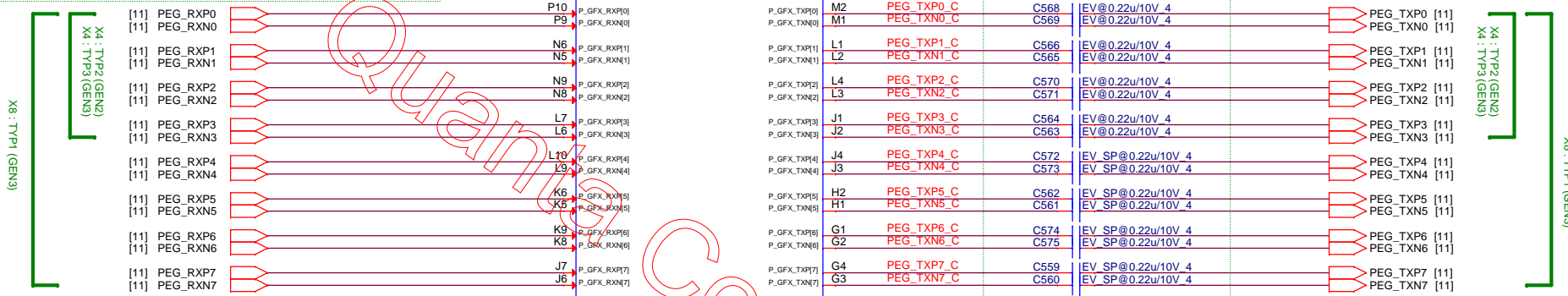
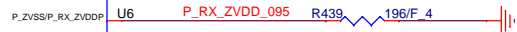


AC-coupling capacitor(depend on GenX, not TYPE)
TYP1&3:(220nF)CH4222K9B04: Only Gen3 and Both of Gen2&3
TYP2 : (100nF)CH4103K1B08: Only Gen2


TYP2 no Gen3



1.05V VDDP only for CZ with DDR-2133 memory
If running DDR-1866 or slower memory,
Platform VDDP should be set to 0.95V
TYP13: (196R_CS11962FB00)
CZL: (1.69K_CS21692FB01)

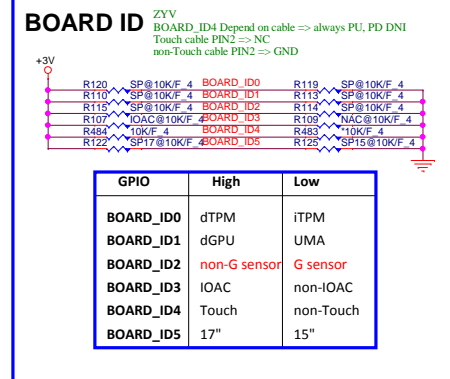
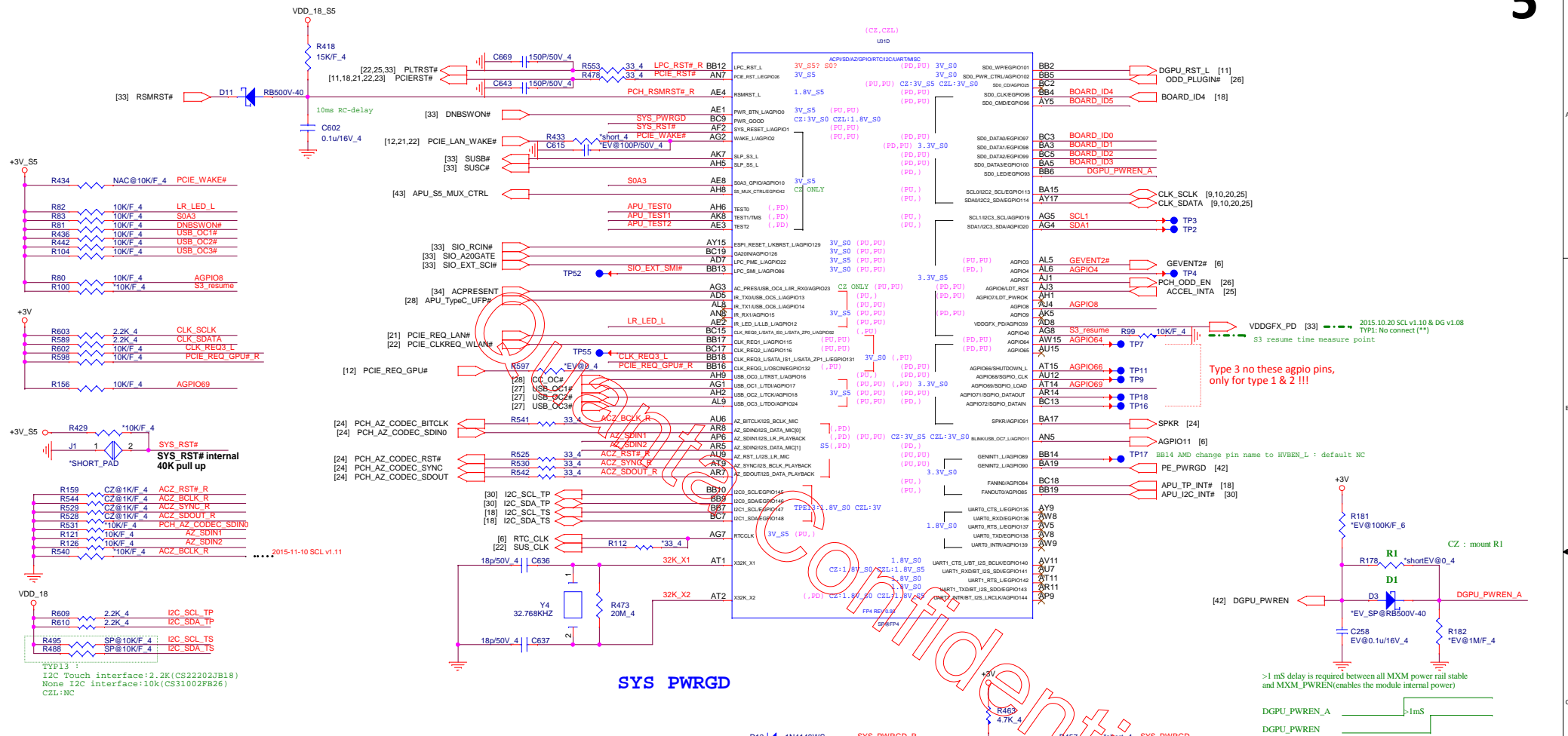


AC-coupling capacitor(depend on GenX, not TYPE)
TYP1&3:(220nF)CH4222K9B04: Only Gen3 and Both of Gen2&3
TYP2 : (100nF)CH4103K1B08: Only Gen2



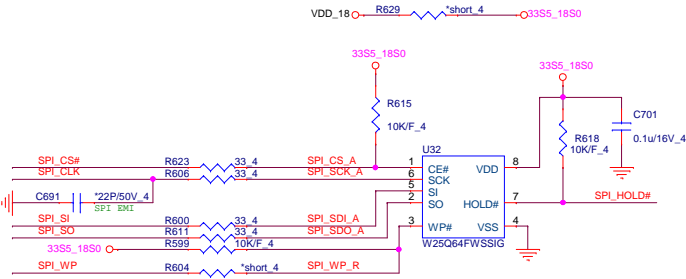
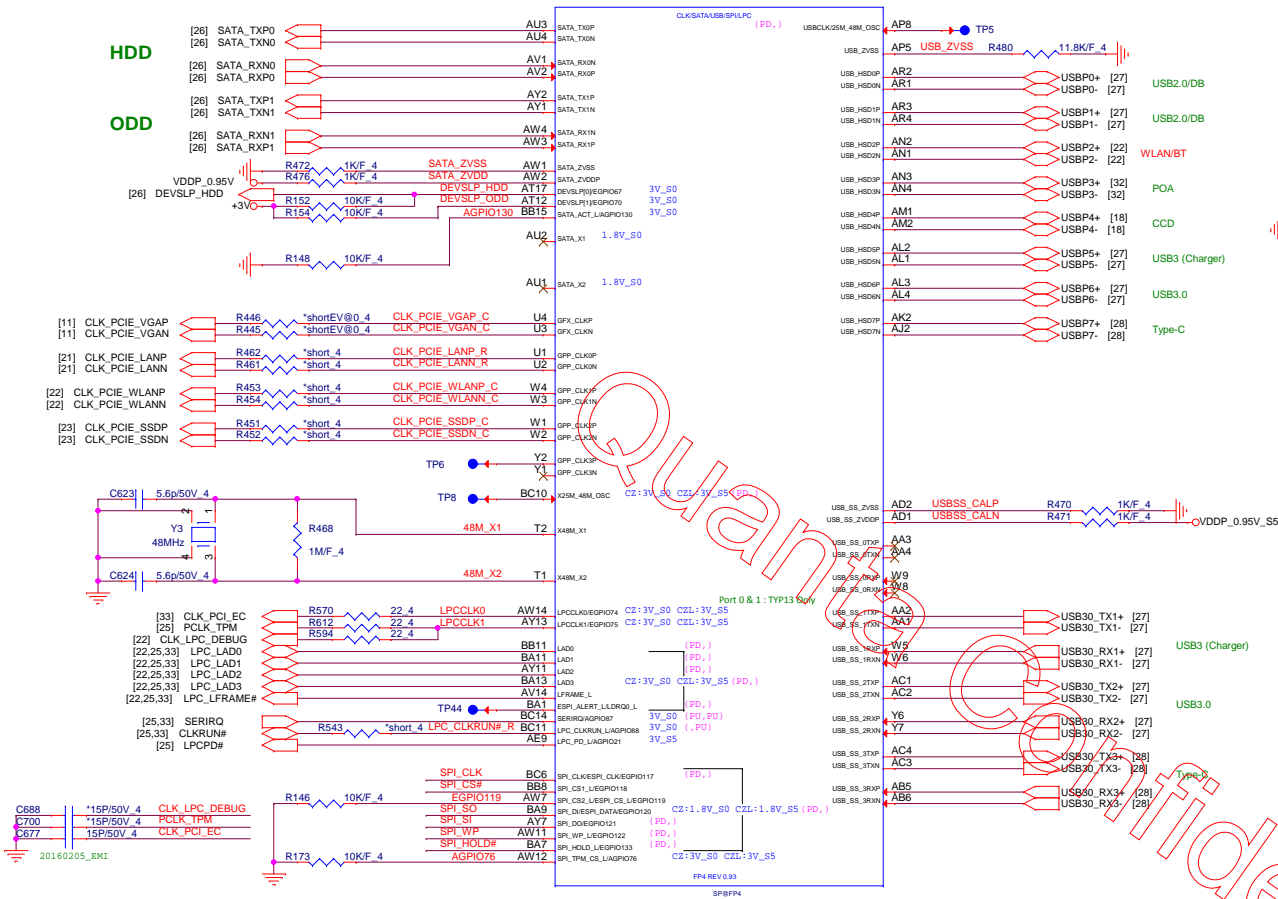
Quanta Computer Inc.
PROJECT : ZAB

Size	Document Number	Rev
	FP4 PCIE I/F(1/7)	1A
Date:	Monday, February 15, 2016	Sheet 2 of 45



HDD

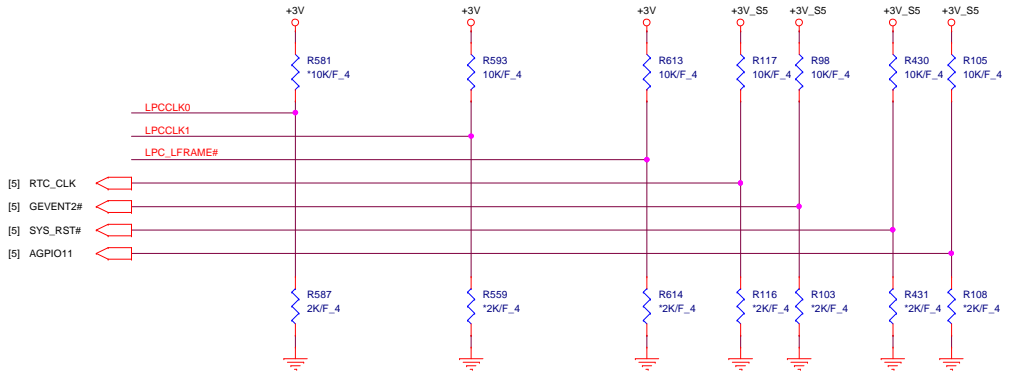
ODD



SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
TYP13 1.8V	WND	8M	AKE5EZNO00	W25Q64FWSSIG
	GGD	8M	AKE5EG-0Q00	GD25LQ64CSIGR
	EON	8M		

STRAPS PINS



	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2# (AGPIO3)		SYS_RST#	AGPIO11(BLINK)
					CZ-L	TYP13		
PU	BOOT Fail Timer ENABLE	Internal CLKGEN	SPI ROM	Coin battery is on board.	1.8V SPI ROM	Enhanced Reset logic	normal reset mode	LDT_RST#/LDT_PWRGD output to APU
		DEFAULT	DEFAULT	DEFAULT		DEFAULT	DEFAULT	DEFAULT
PD	BOOT Fail Timer DISABLE	External CLKGEN	LPC ROM	Coin battery isn't on board.	3.3V SPI ROM	Traditional Reset logic	short reset mode	LDT_RST#/LDT_PWRGD output to Pads
	DEFAULT				DEFAULT			

22 uF * 8
0.22 uF * 6
180 pF * 1

10 uF * 4
0.22 uF * 6
180 pF * 1

22 uF * 9
0.22 uF * 8
180 pF * 1

22 uF * 9
0.22 uF * 9
180 pF * 1

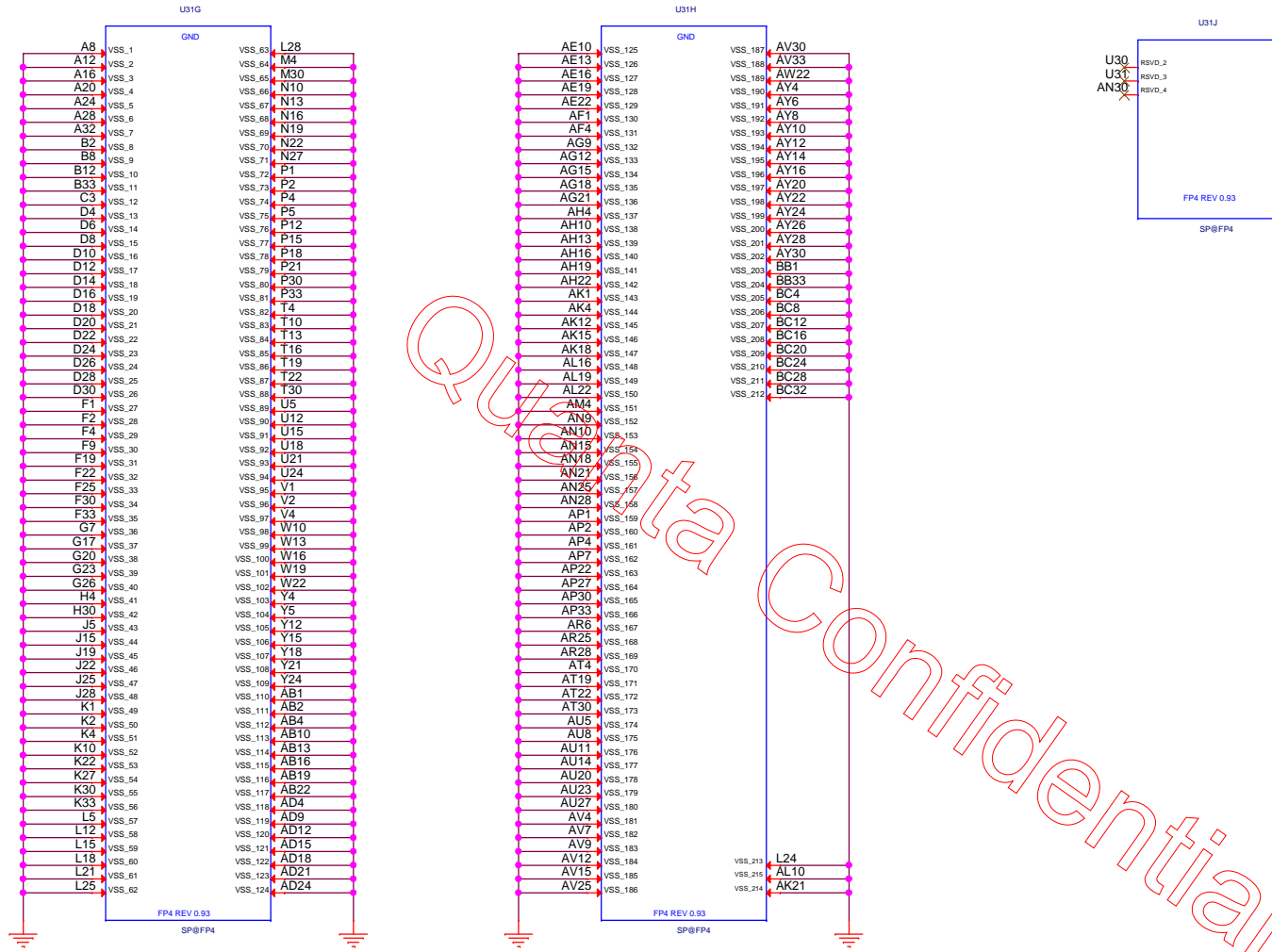
22 uF * 4
0.22 uF * 8
180 pF * 1

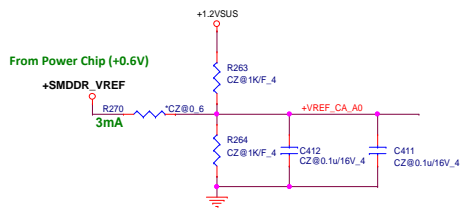
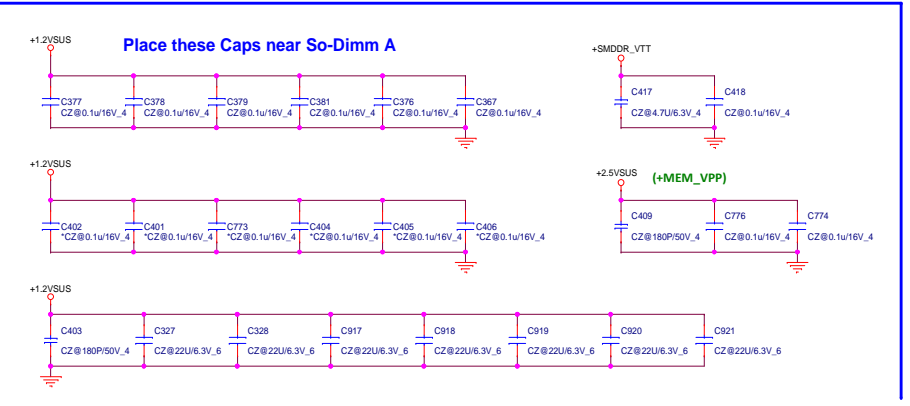
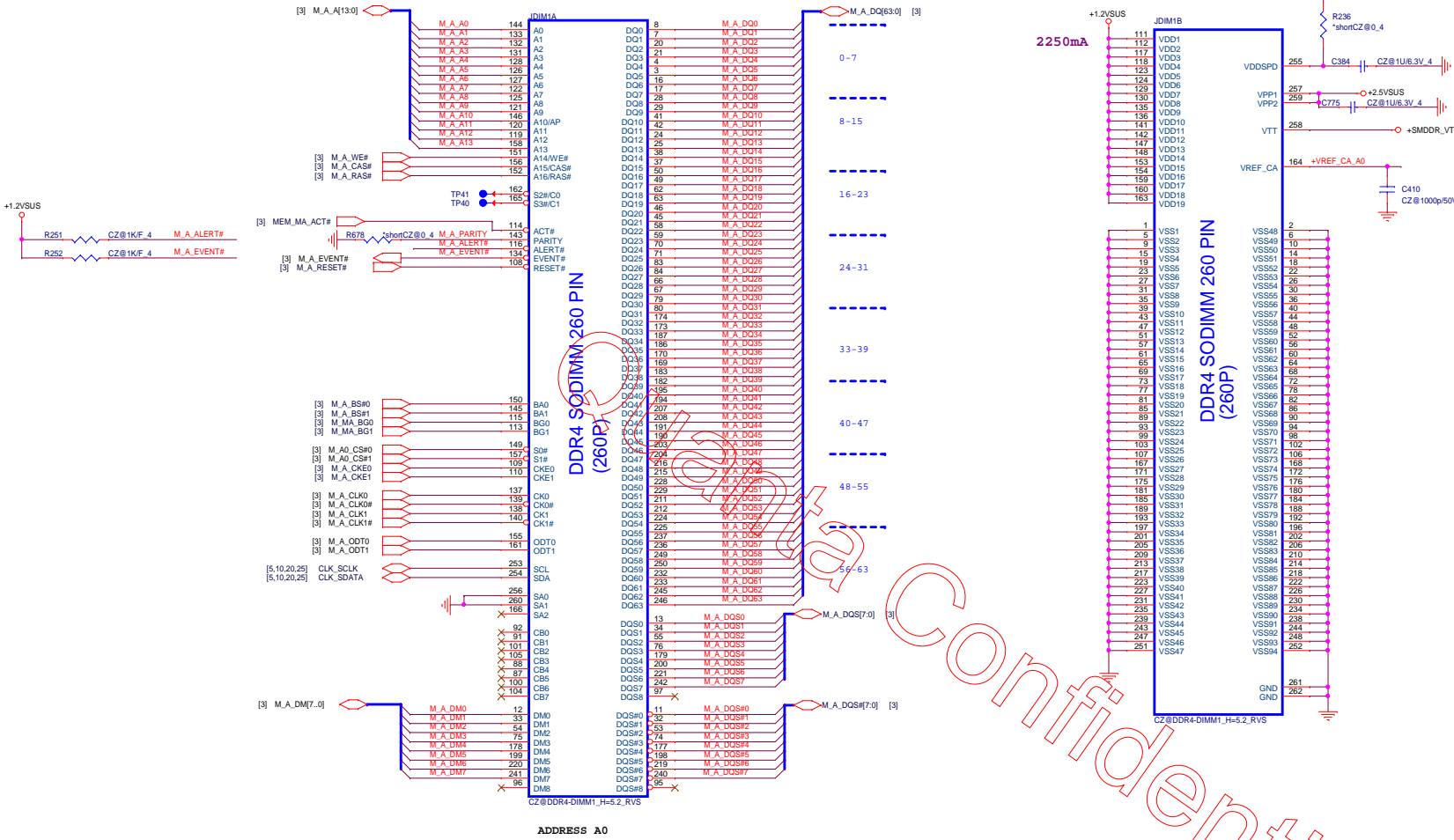
RTC (RTC)

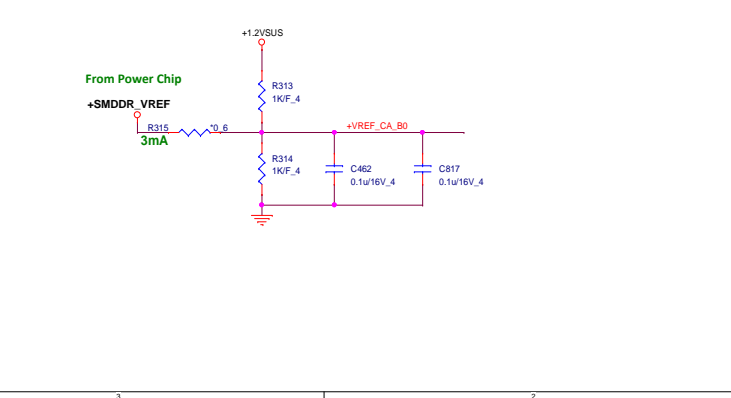
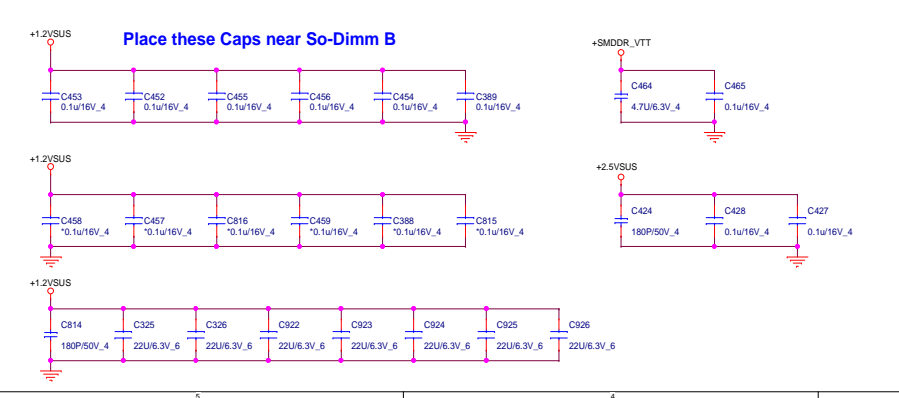
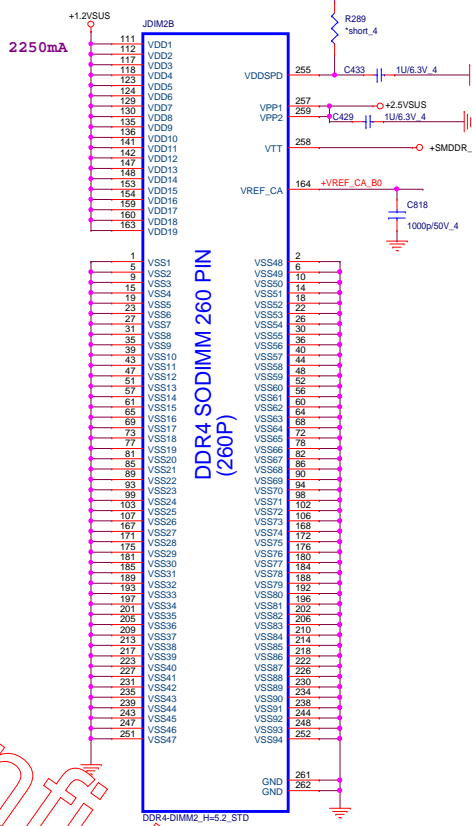
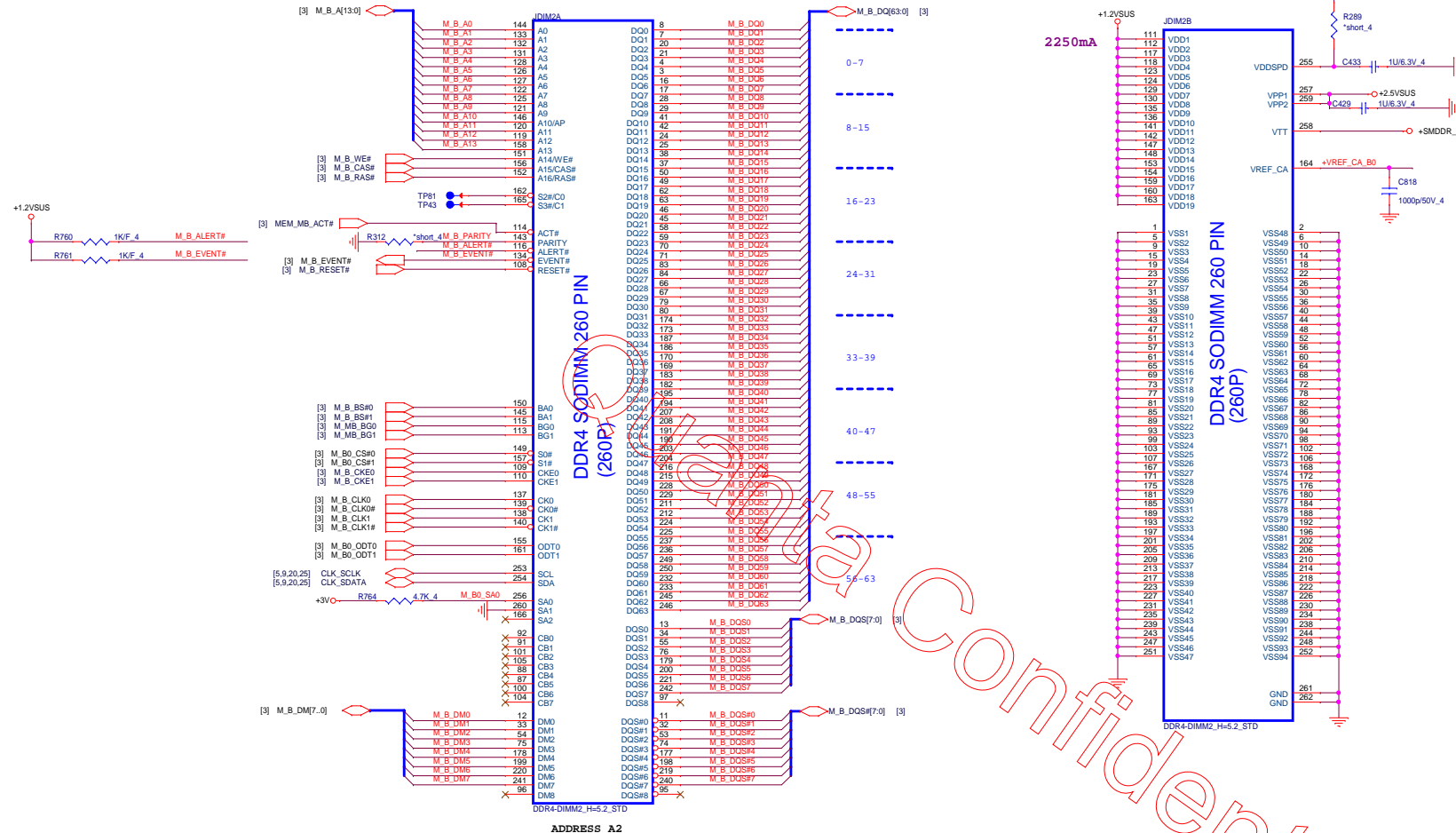
For EC reset RTC

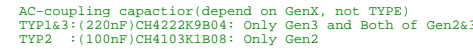
[33] CLR_CMOS

RTC CR2032 Coin Battery
DBV: AHL03003057
VDE: AHL03003003
JHT: AHL03003035

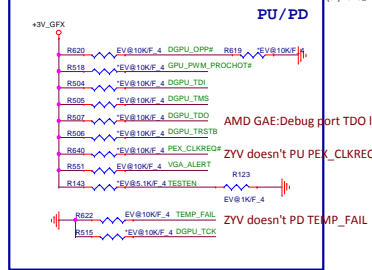
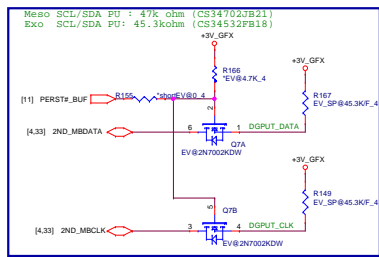




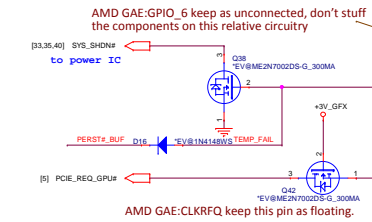




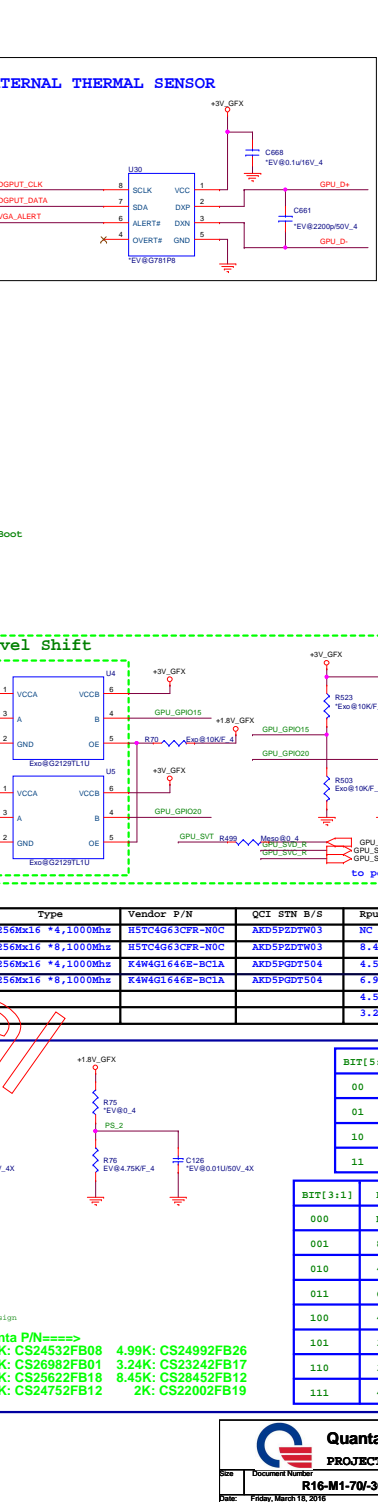
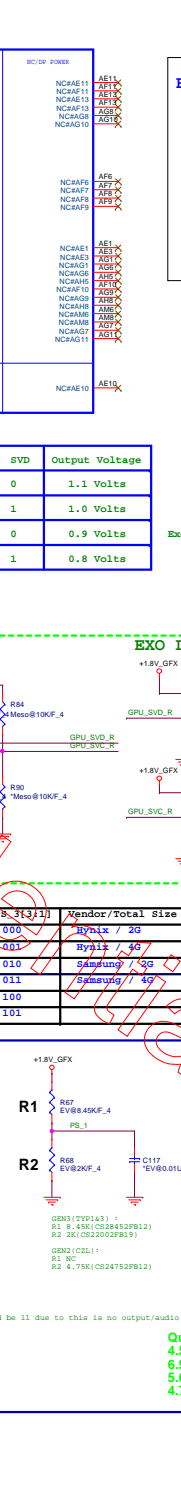
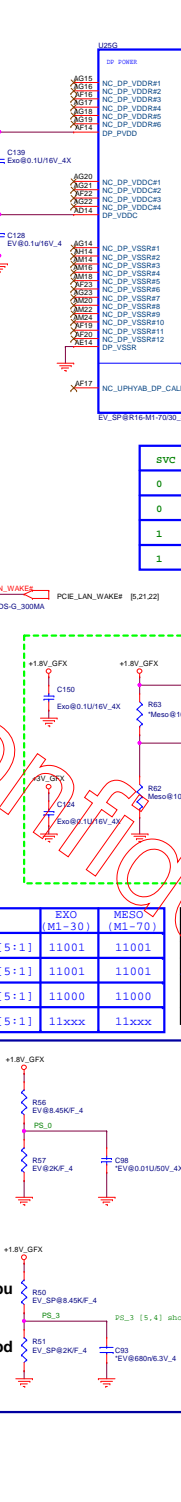
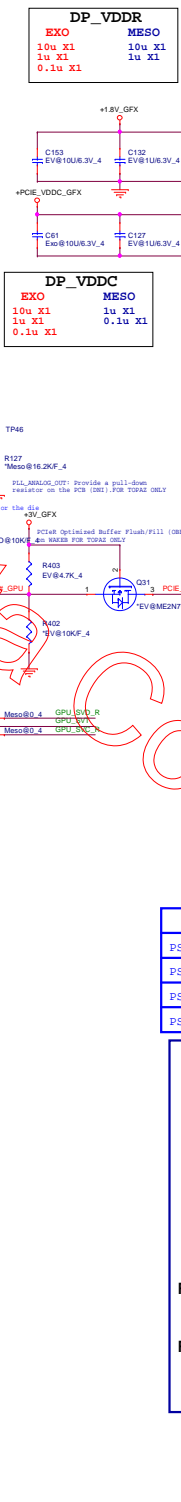
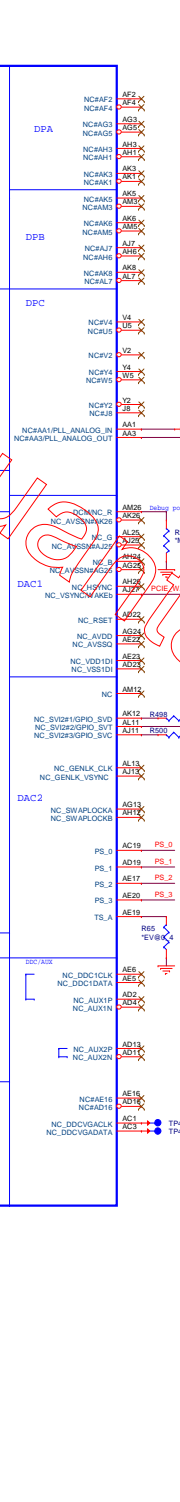
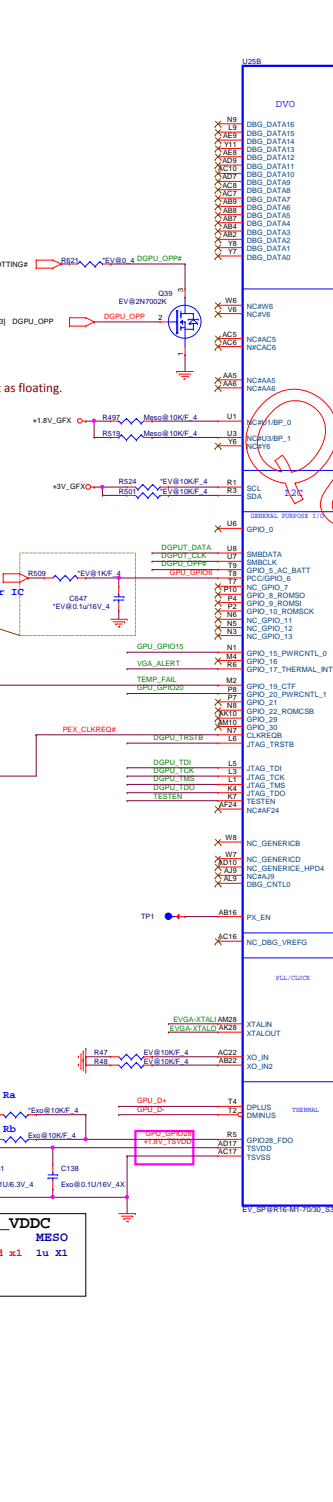
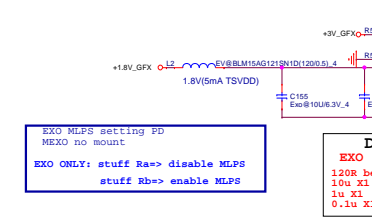
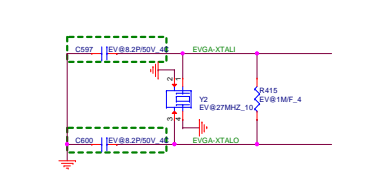
(VGA)
The SMBus slave ID is default 0x41



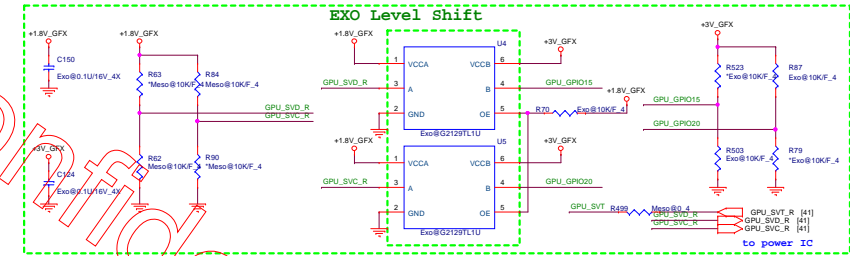
Peak Current Control (PCC) GPIO_6.
FOR MESO ONLY



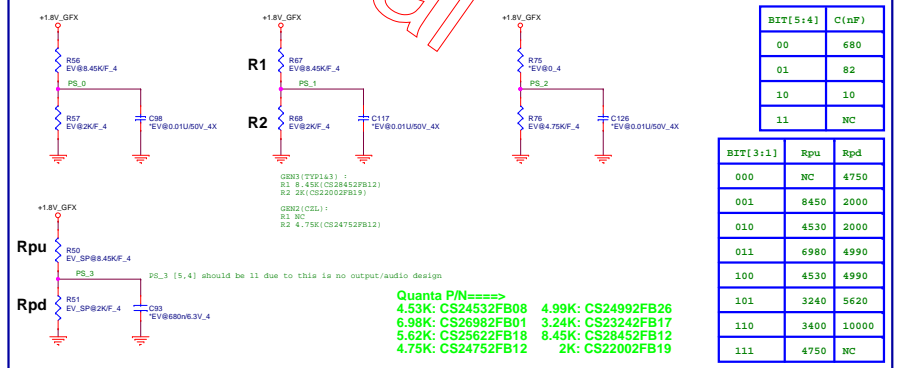
GPIO_11, 12, and 13 FOR MESO ONLY,
EXO become NC

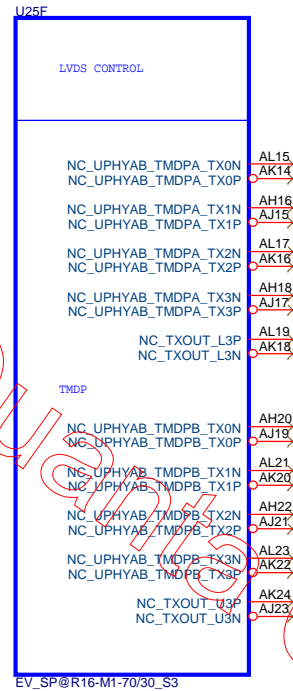
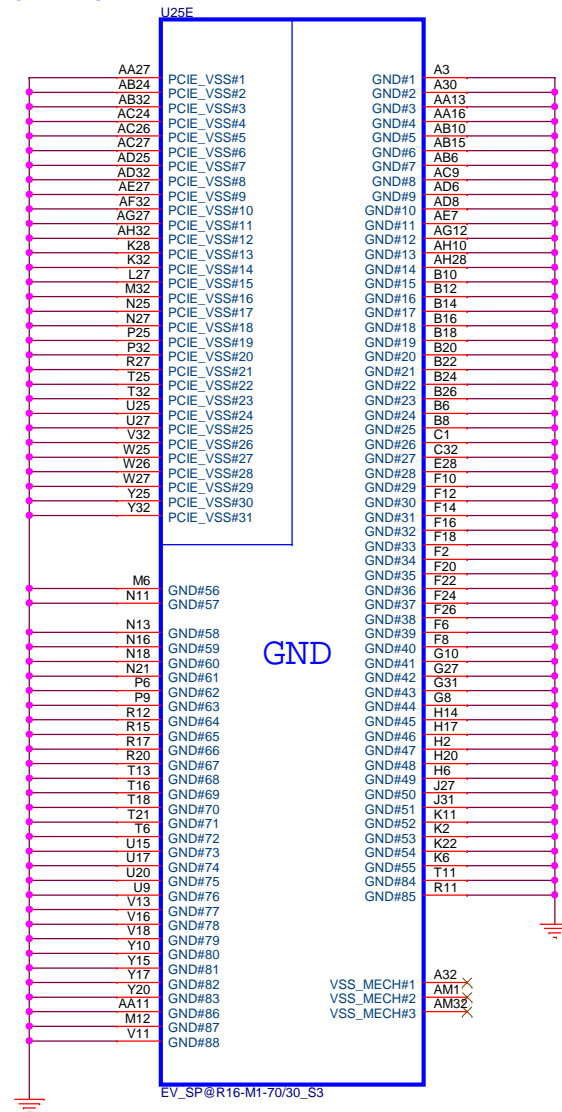


SVC	SVD	Output Voltage
0	0	1.1 Volts
0	1	1.0 Volts
1	0	0.9 Volts
1	1	0.8 Volts



	EXO (M1-30)	MESO (M1-M70)	PS (3:1)	Vendor/Total Size	Type	Vendor P/N	QCI STN B/S	Ru	Rpd
			000	Hyllix / 2G	256Mx16 *4,1000MHz	H5TC4G63CFR-NOC	AKD5PD2TW03	KPC	4.75K
PS0[5:1]	11001	11001	001	Hyllix / 2G	256Mx16 *8,1000MHz	H5TC4G63CFR-NOC	AKD5PD2TW03	8.45K	2K
PS1[5:1]	11001	11001	010	Samsung / 4G	256Mx16 *4,1000MHz	K4W4G1646E-BC1A	AKD5PDGT504	4.53K	2K
PS2[5:1]	11000	11000	011	Samsung / 4G	256Mx16 *8,1000MHz	K4W4G1646E-BC1A	AKD5PDGT504	6.98K	4.99K
			100					4.53K	4.9K
PS3[5:1]	11xxxx	11xxxx	101					3.24K	5.62K



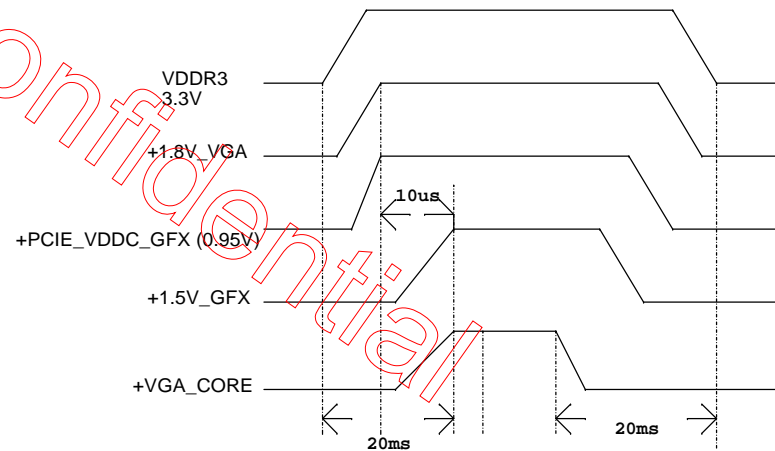


All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

For power down, reversing the ramp-up sequence is recommended.

Power Up/Down Sequence



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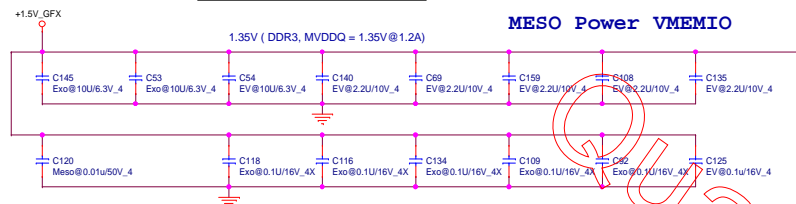
PROJECT : ZAB

Size	Document Number	Rev
	R16-M1-70/30_S3_GND/LVDS/Strap(3/7)	1A

Date: Friday, March 18, 2016 Sheet 13 of 45

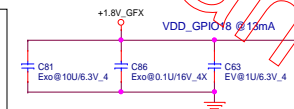
VDDR1	
EXO	MESO
10u X3	10u X1
2.2u X5	2.2u X5
0.1u X6	0.1u X1
	0.01u X1

PCIE_PVDD	
EXO	MESO
10u X1	10u X1
1u X1	1u X1
0.1u X1	
0.01u X1	



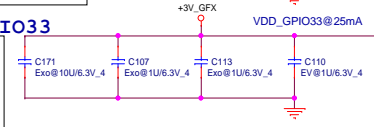
Meso Power VDD_GPI018

VDD_CT	
EXO	MESO
bead 120 X1	1u X1
10u X1	
0.1u X1	

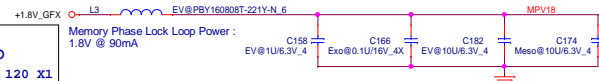


Meso Power VDD_GPI033

VDDR3	
EXO	MESO
bead 120 X1	1u X1
10u X1	
1u X3	



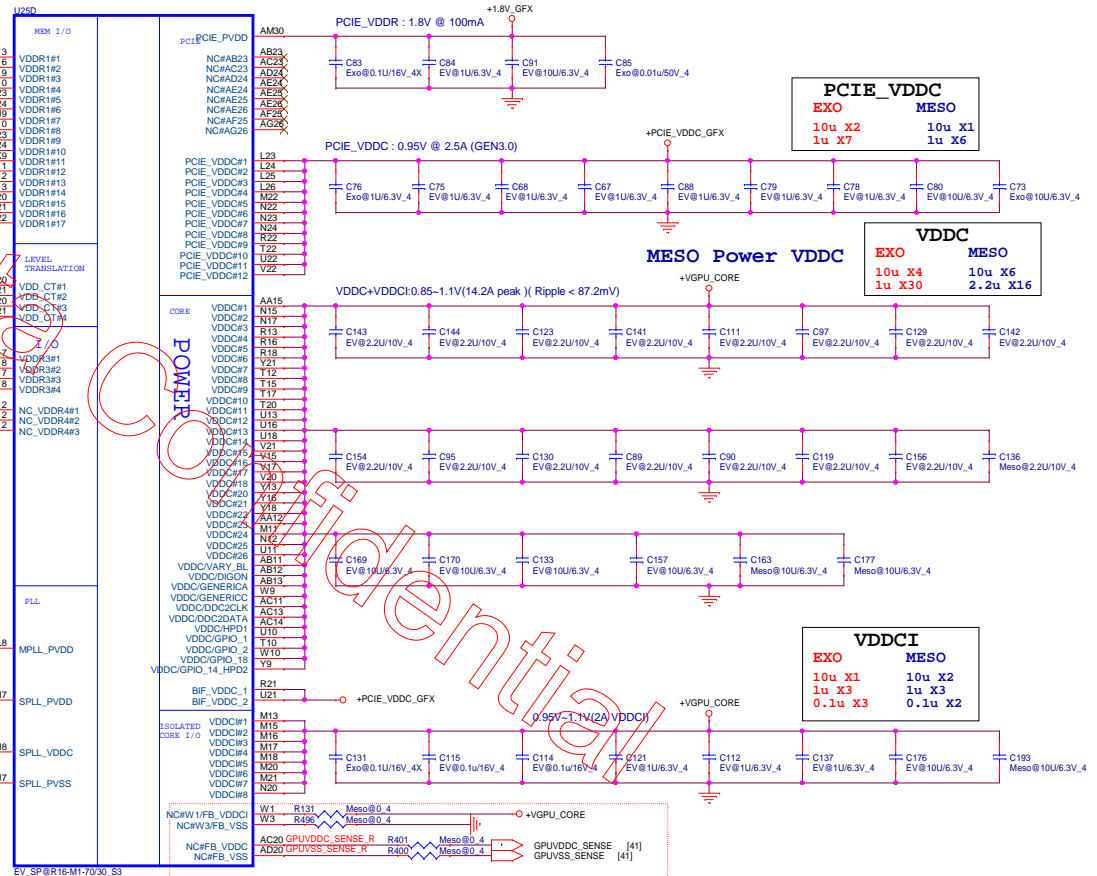
MPLL_PVDD	
EXO	MESO
bead 220 X1	bead 220 X1
10u X1	10u X2
1u X1	1u X1
0.1u X1	



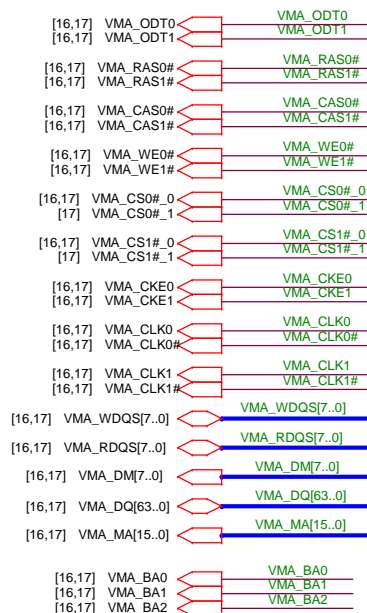
SPLL_PVDD	
EXO	MESO
bead 120 X1	bead 120 X1
10u X1	1u X1
1u X1	10u X1
0.1u X1	



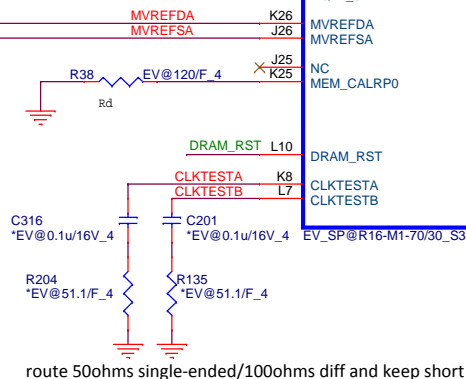
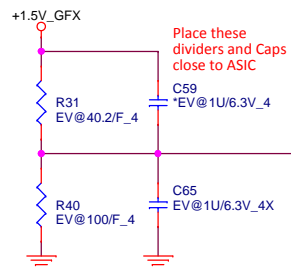
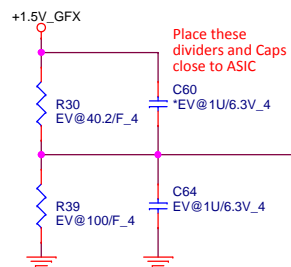
SPLL_VDDC	
EXO	MESO
bead 120 X1	bead 120 X1
10u X1	1u X1
1u X1	0.1u X1
0.1u X1	



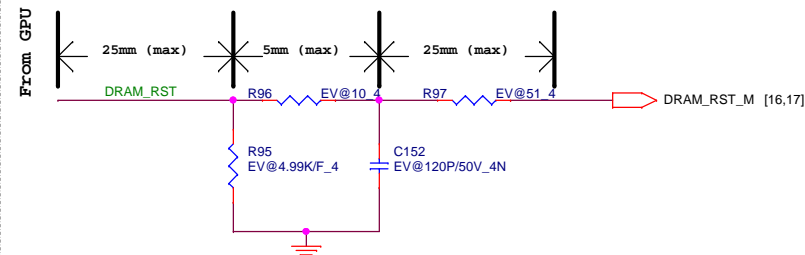
EXO doesn't support this function
(refer to GPU SCL)



To support 2/4 Gbits VRAM,
dual Rank
(256 Mbits X 16 x 4/8 pcs)



MEMORY INTERFACE



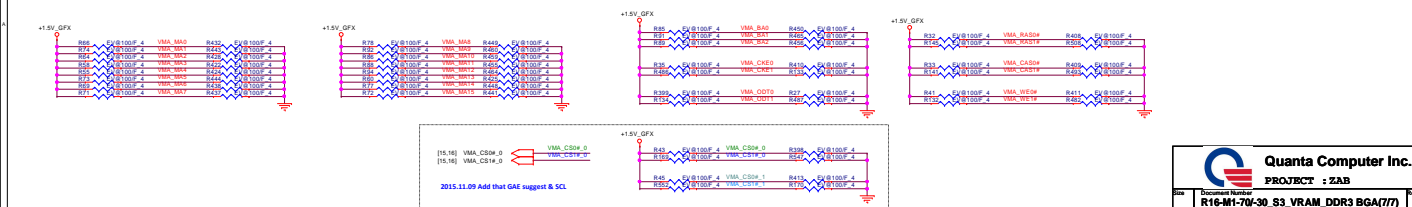
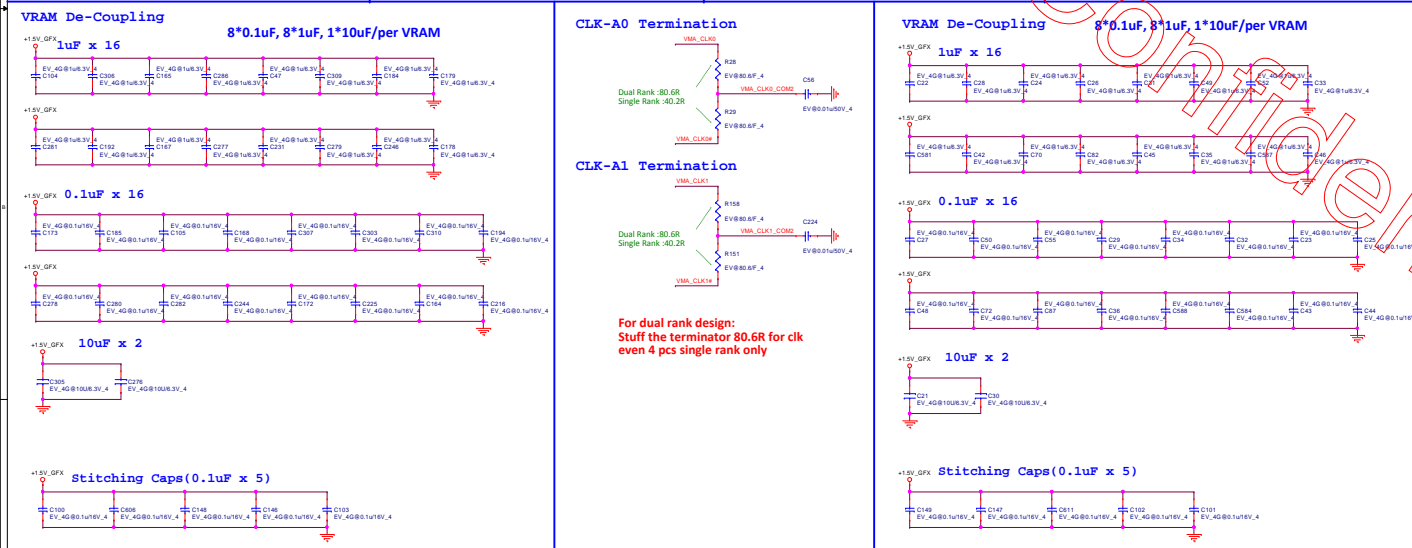
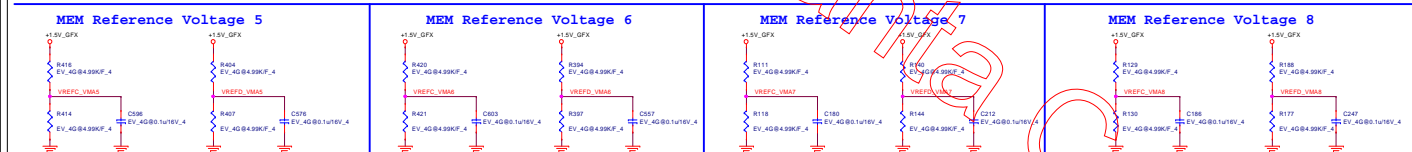
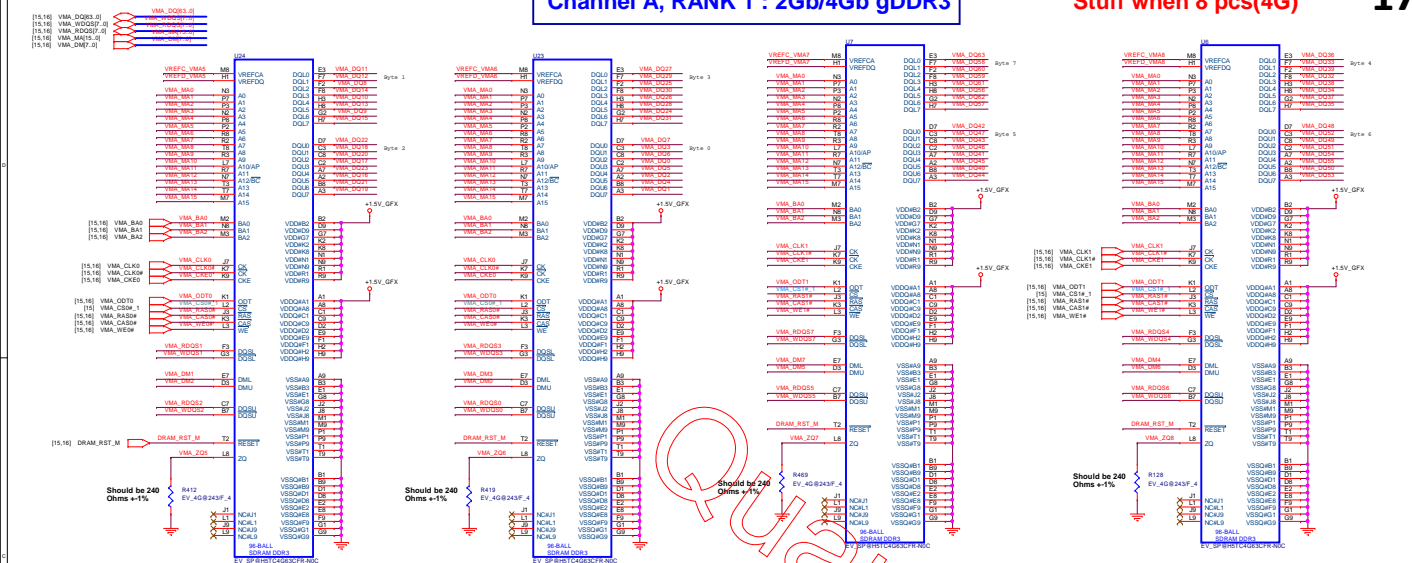
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

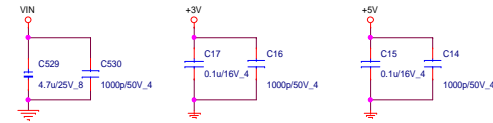
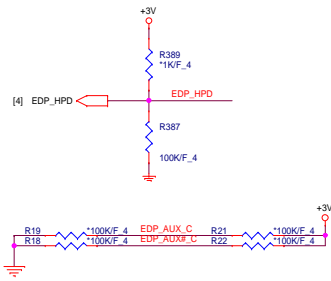


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PROJECT : ZAB

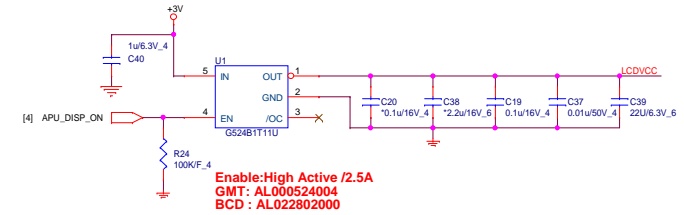
Size	Document Number	Rev
	R16-M1-70-30_S3_MEM(5/7)	1A
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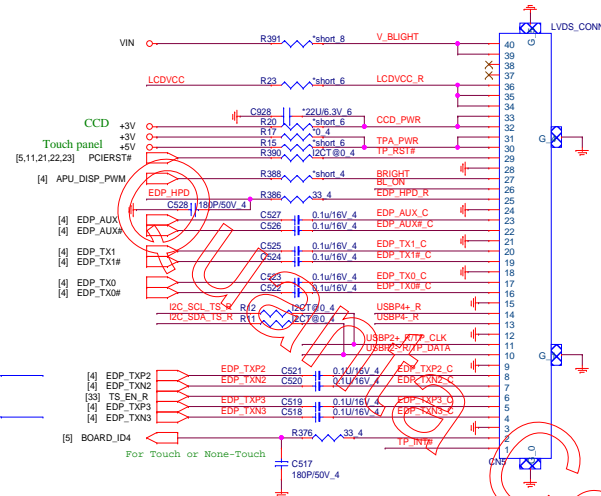
LCD (LDS)



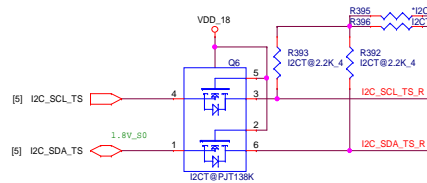
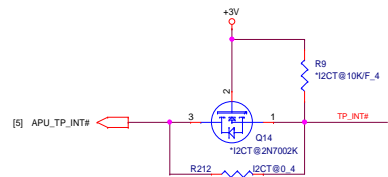
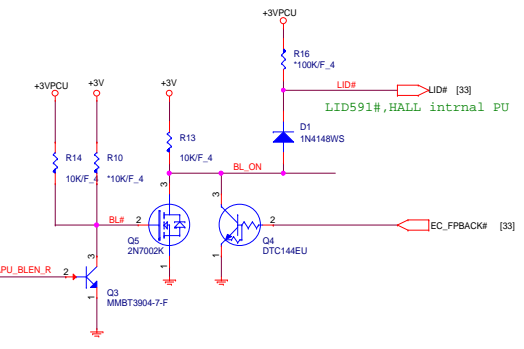
LCD Power (LDS)



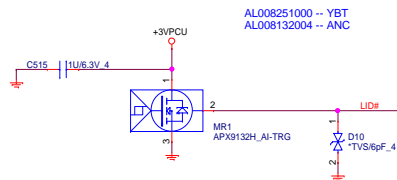
Front Camera (FCM)



Backlight Control (LDS)



Lid Switch (HSR)



4Kx2K (HDM)

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	Source active	Active mode: DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



Add it when using HDMI level shifter



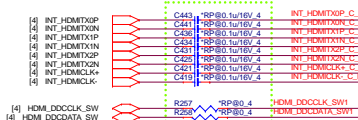
Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V _{DD}	2 dB
short to V _{DD}	short to GND	4 dB
short to V _{DD}	short to V _{DD}	6 dB



From APU

Co-Layout



Co-Layout



Co-Layout



Co-Layout

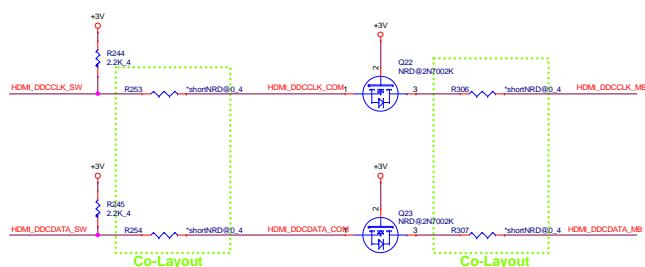


To Choke



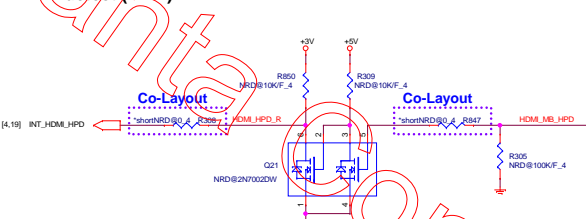
HDMI DDC (HDM)

Normal Rout

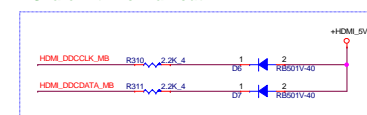


HDMI-detect (HDM)

Normal Rout



**Share with normal rout



HDMI(HDM)

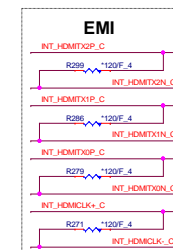
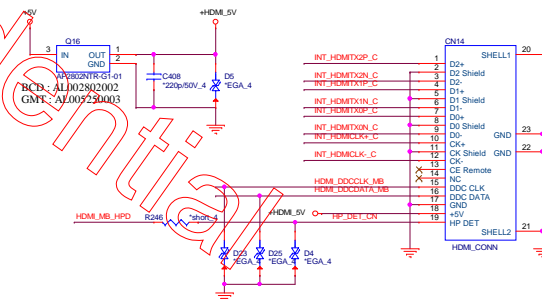
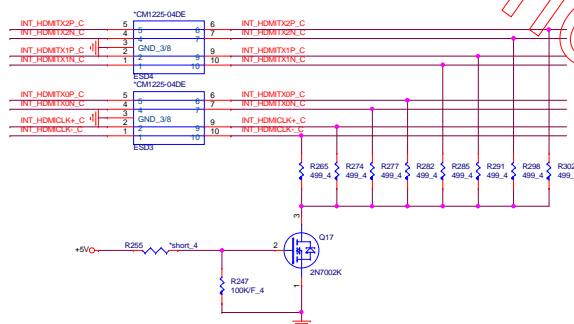
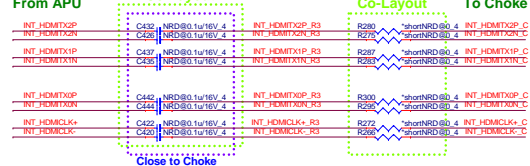
Normal Rout

From APU

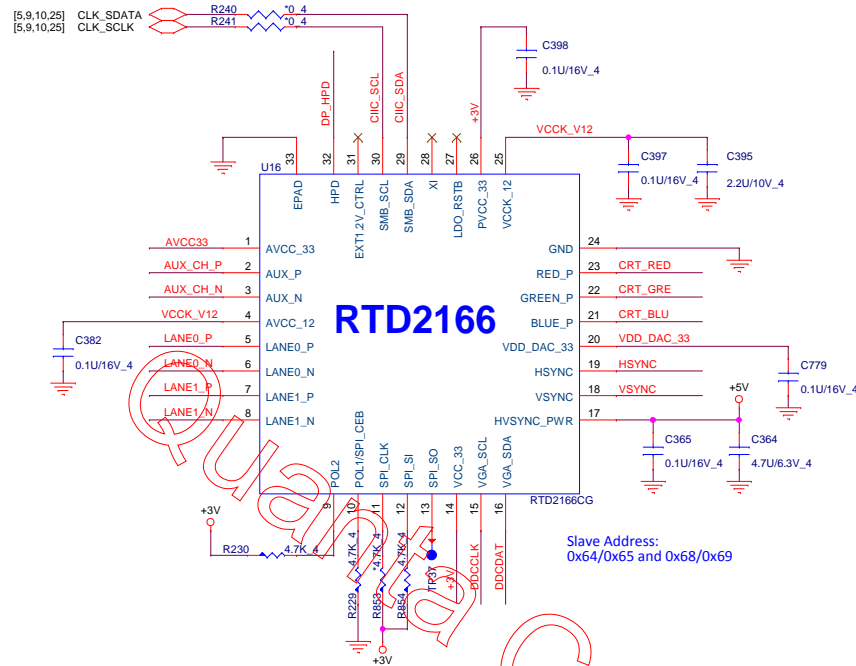
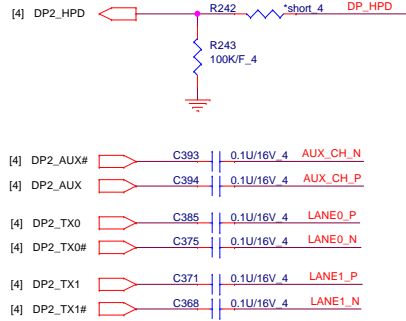
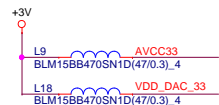
Co-Layout

Co-Layout

To Choke



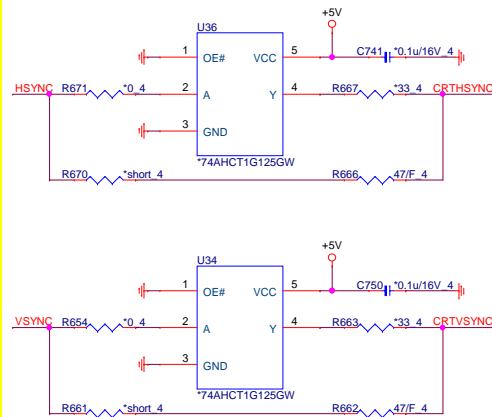
Power



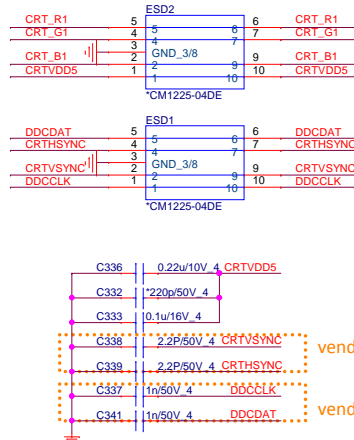
Note:

- 1- Caps should be placed close to chip
- 2- Pin 9's Cap should be X5R material
- 3- R,G,B's R should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

RTD2166 integrate 5V HSYNC/VSYNC buffer inside IC
Reserved for debug

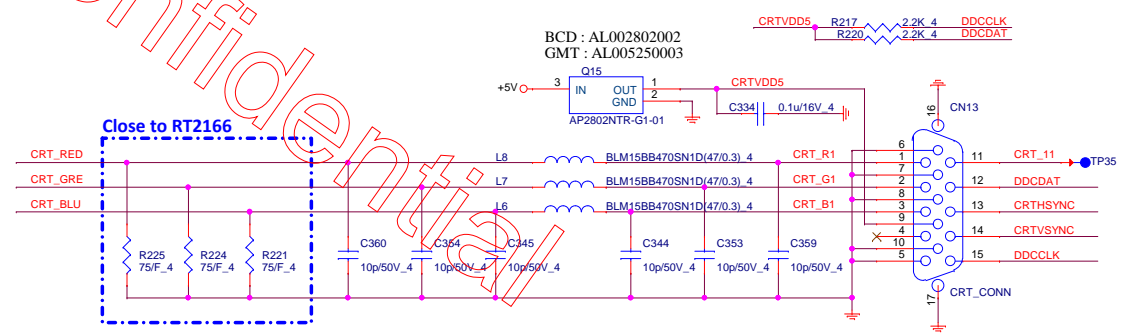


Co-Layout



vendor test report

vendor projector result

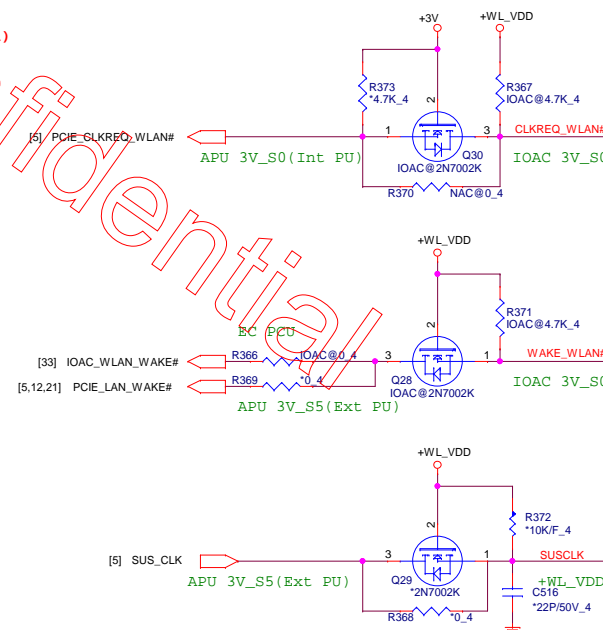
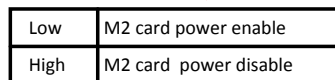


Quanta Computer Inc.

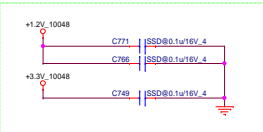
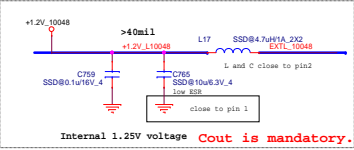
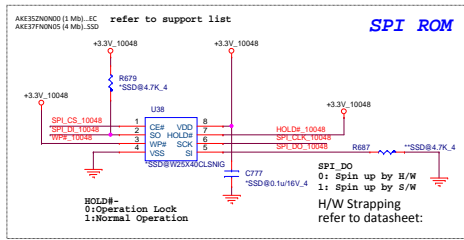
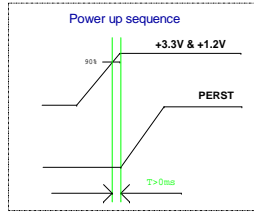
PROJECT : ZAB

Size	Document Number	Rev
	CRT/DP2VGA(RTD2166)	1A

Date: Monday, March 07, 2016 Sheet 20 of 45



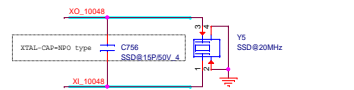
PCIe to SATA III (HDD)



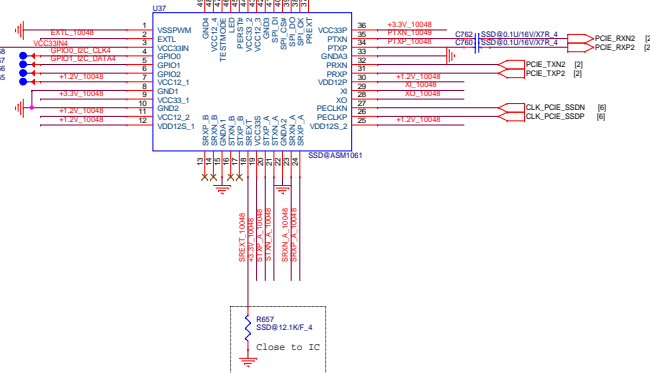
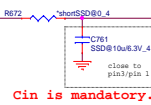
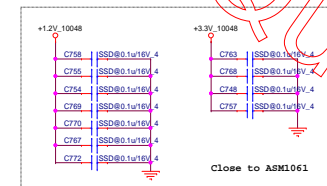
Delete...
Just choose one of external 1.25V regulator or IC internal regulator (@Pin Z).

Option; refer to datasheet or contact FAE

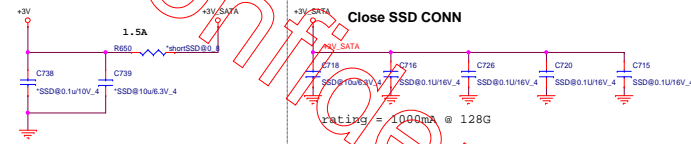
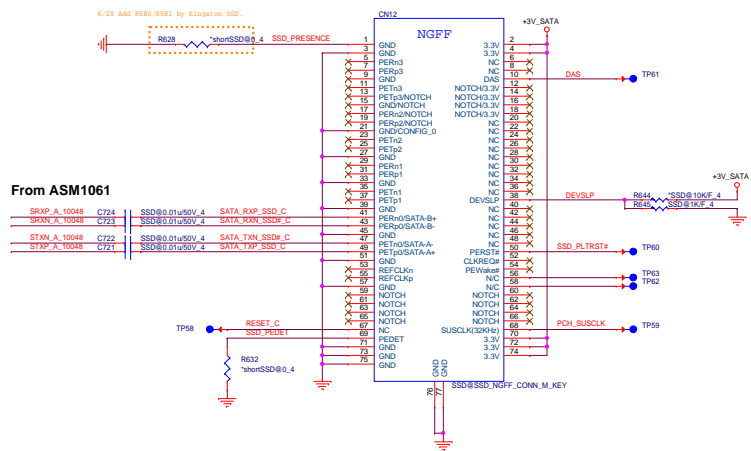
Frequency Tolerance: +/-30PPM
CL: 20pf



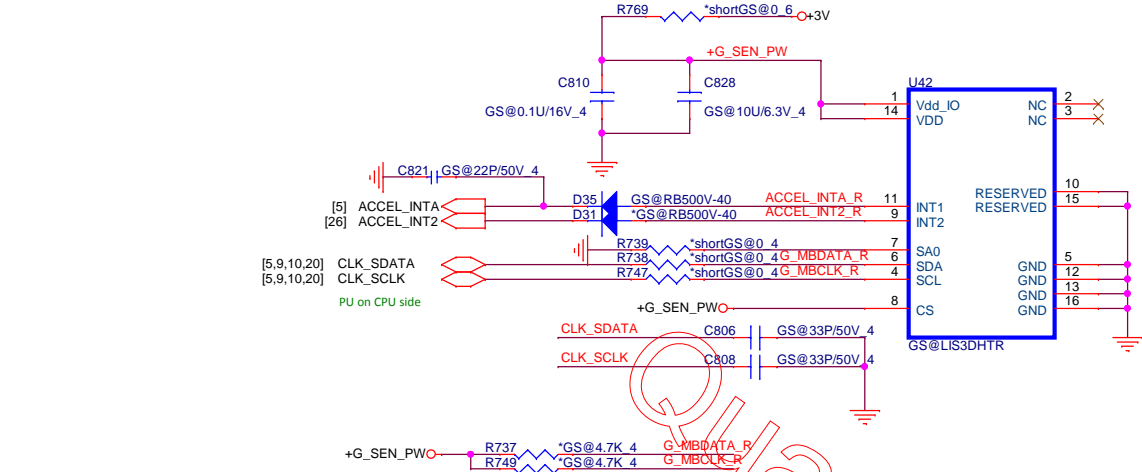
XTAL-GA-B0 type



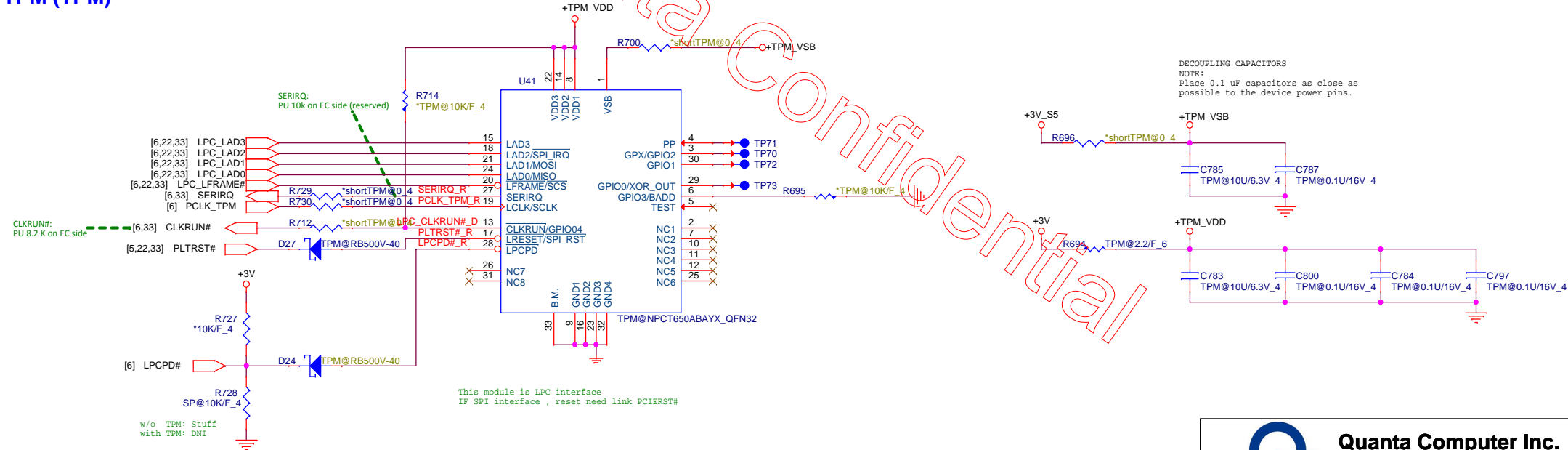
NGFF_M.2 SSD (NGF)

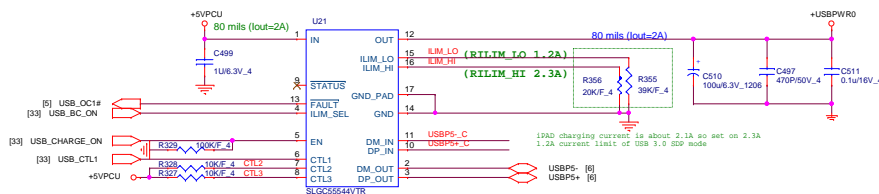


pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated.
10	DAS#	Device Activity Signal
21	WMAN/SSDIND_N	This pin connect to Ground
38	Device sleep signal	If system didn't support DEVSLP, set DEVSLP sleep signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP sleep signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MPG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MPG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IFDET	This pin connect to Ground



TPM (TPM)





GMT:AL003703000(G3703)_X
TI:AL002544001(TPS2544)
Silerqy:AL055544000(SLGC55544VTR)

	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RTLIM IO is optional and the ILM IO pin may be left unconnected if the following conditions are met:

- RILIM_LO is optional and the RILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
 2. Load Detection - Port Power Management is not used
 3. Mouse / Keyboard wake function is not used
- If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

The following equation programs the typical current limit:

(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$\text{IOS_typ(mA)} = 50,250 / \{\text{RILIM_XX(K}\Omega\text{)} + 0.1\}$$

USB 3.0 redriver (UB3)

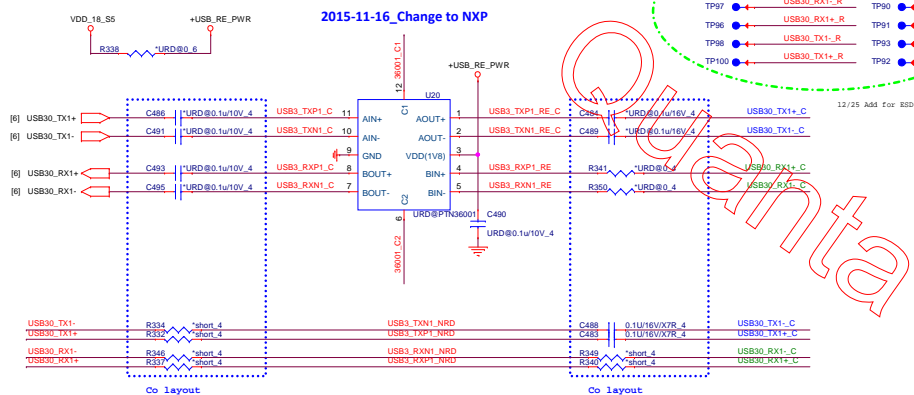


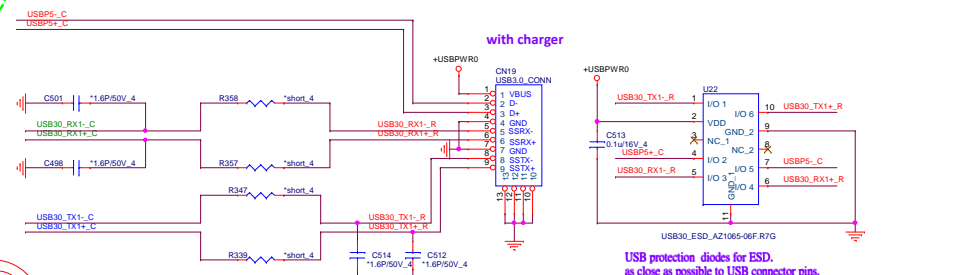
Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ ^[1]	DE ^[2]	OS ^[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

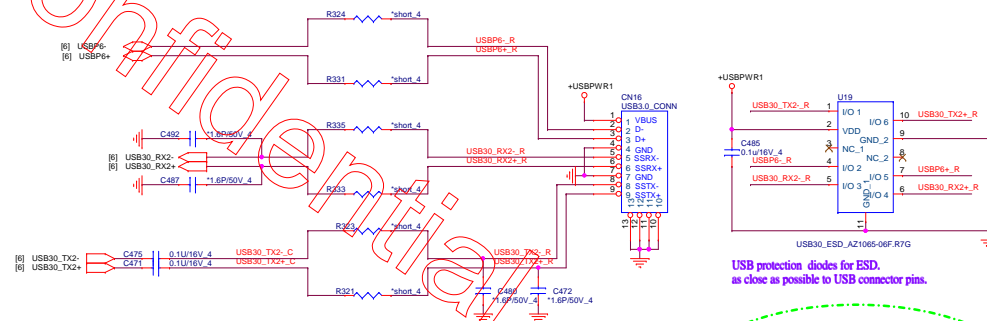
Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ ^[1]	DE ^[2]	OS ^[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

USB 3.0 Connector (UB3)

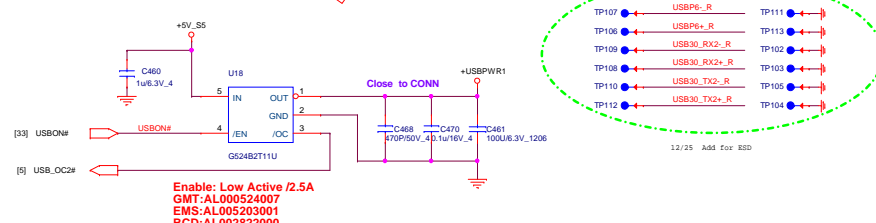
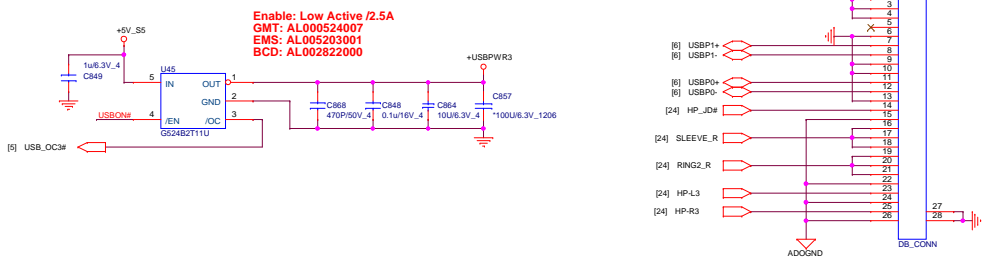


USB protection diodes for ESD,
as close as possible to USB connector pins.



USB protection diodes for ESD,
as close as possible to USB connector pins

DB
USB2.0 (UB2)



Enable: Low Active /2.5A
GMT:AL000524007
EMS:AL005203001
BCD:AL002822000

USB 3.0 redriver

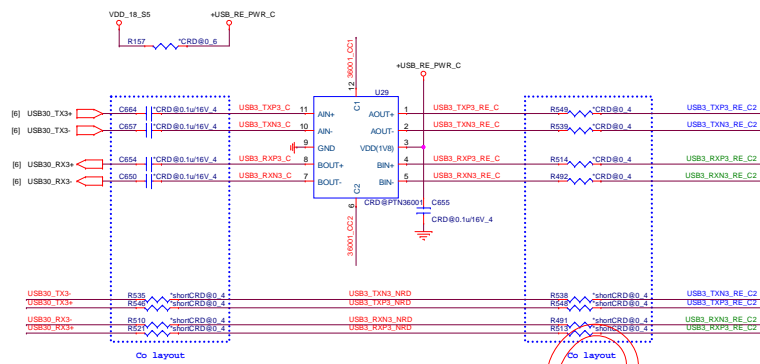
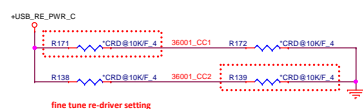


Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

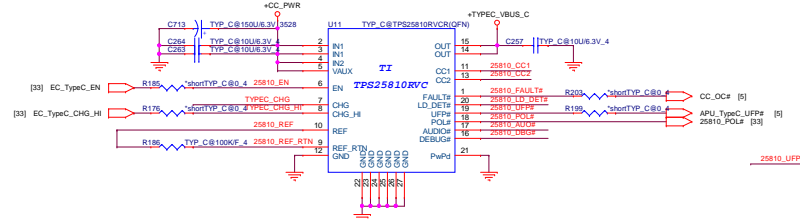
Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ ^[1]	DE ^[2]	OS ^[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

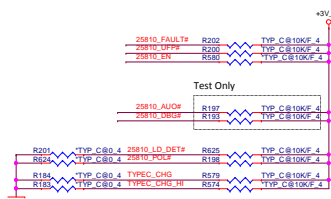


Type-C CC

Vendor suggest input cap 120u

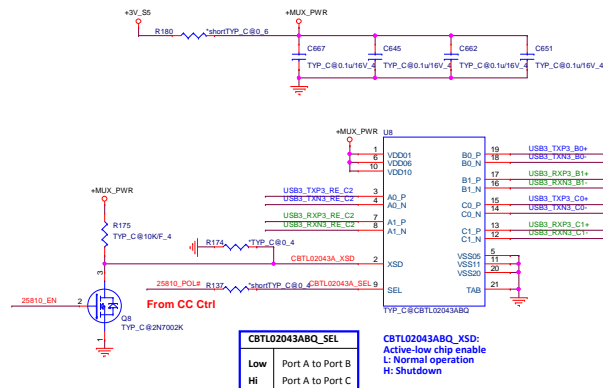


CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



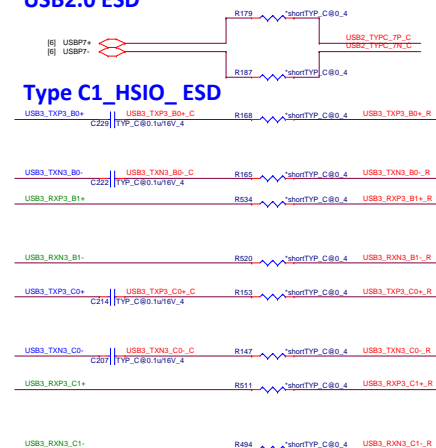
TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

Type-C MUX

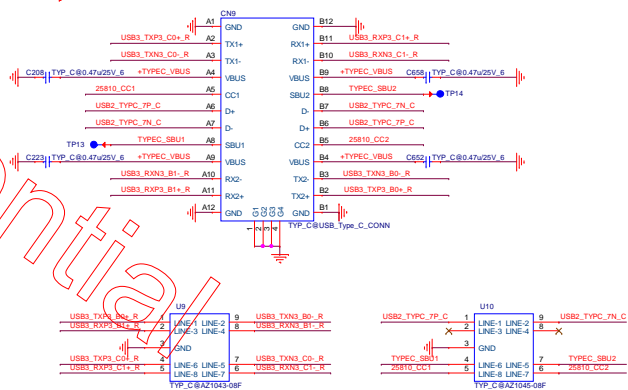


USB2.0 ESD

Close to connector



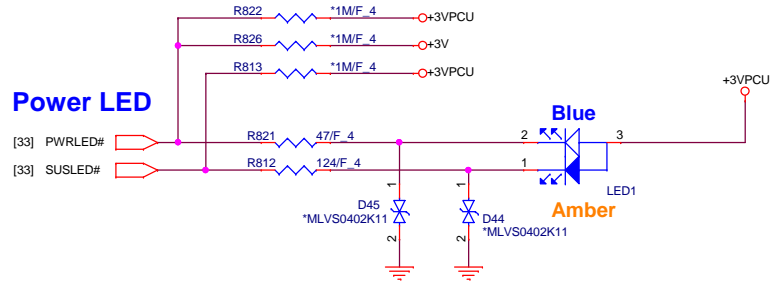
Type C1_HSIO_ESD



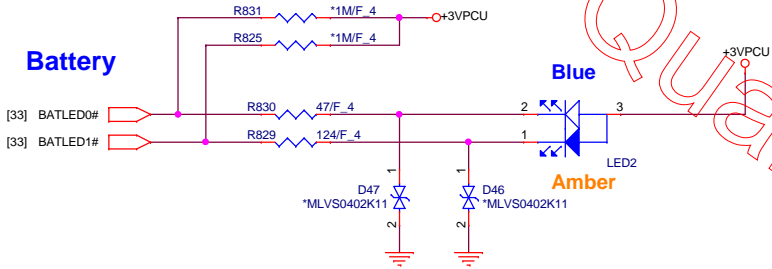
Quanta P/NAMAZING P/NUSD保護位置
BC104308Z00, AZ1043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00, AZ1045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00, AZ5725-01F.R7G0.009 PD 5V (follow ZAA)

LED(UIF)

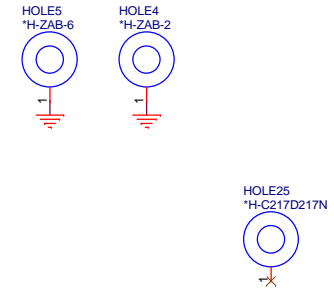
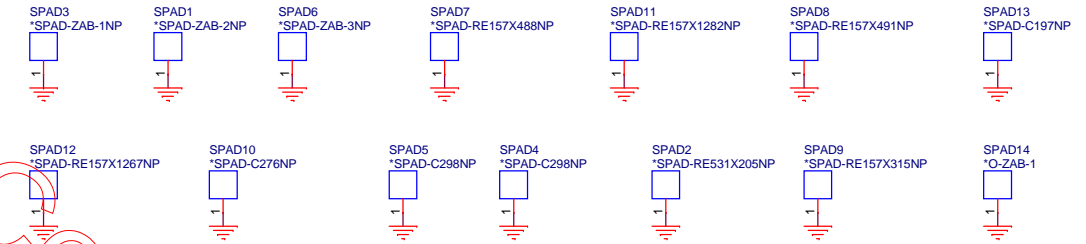
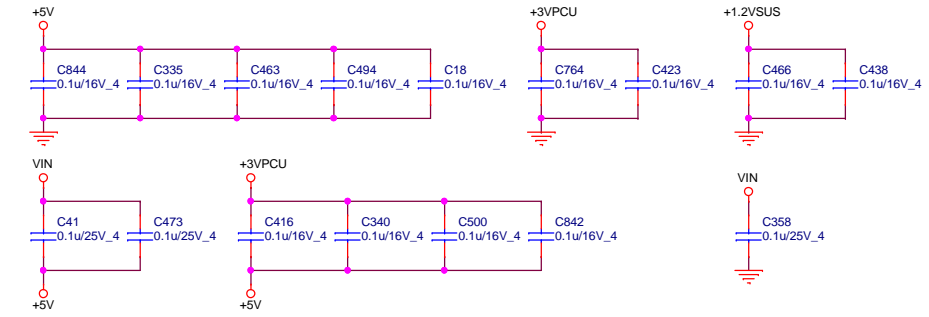
Power LED



Battery

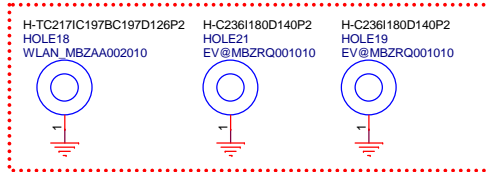


Stich cap

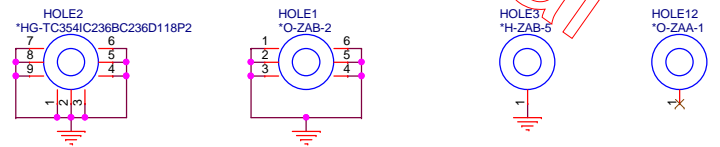
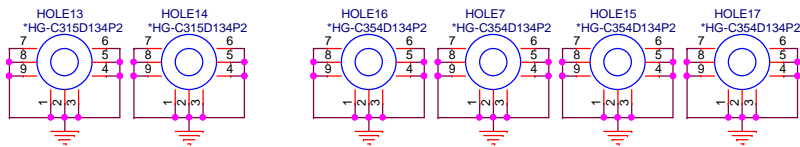
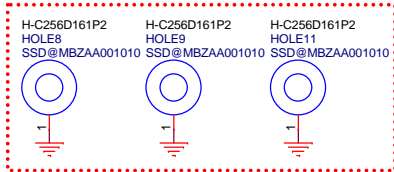



HOLE(OTH)

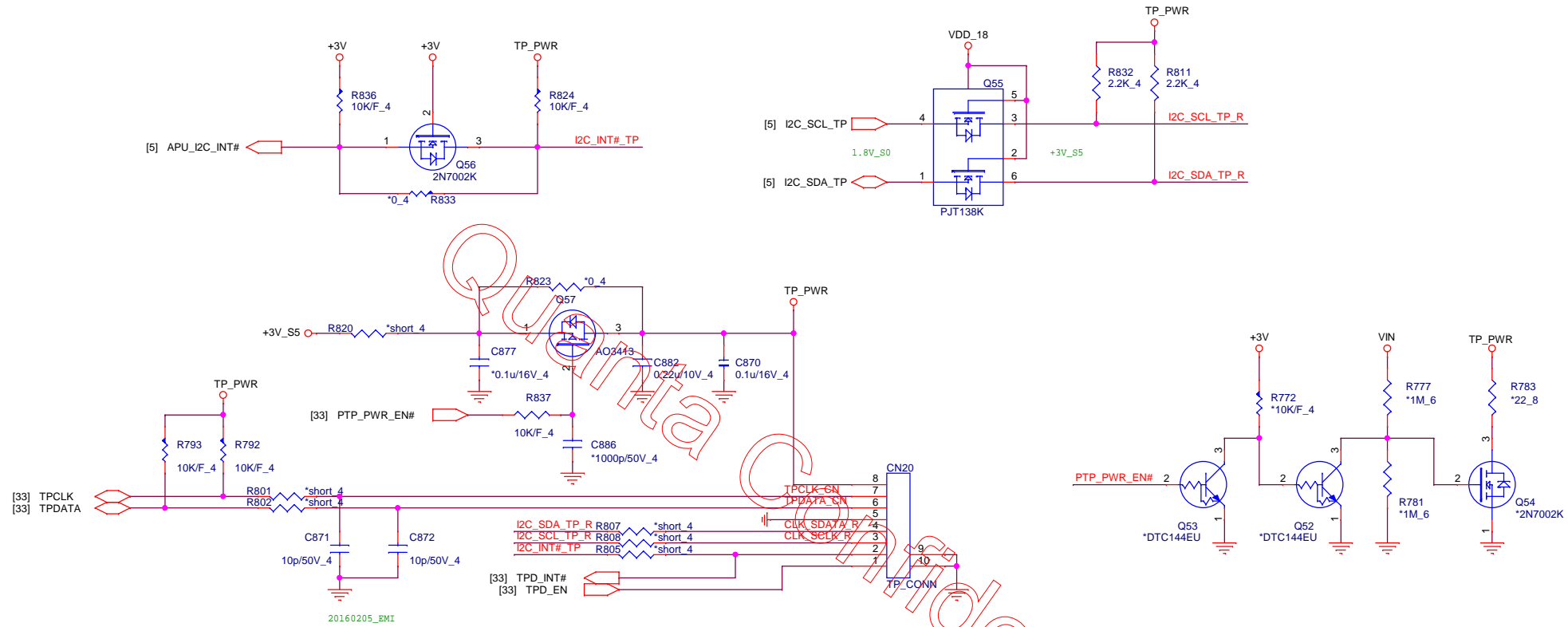
Layout set on Bottom



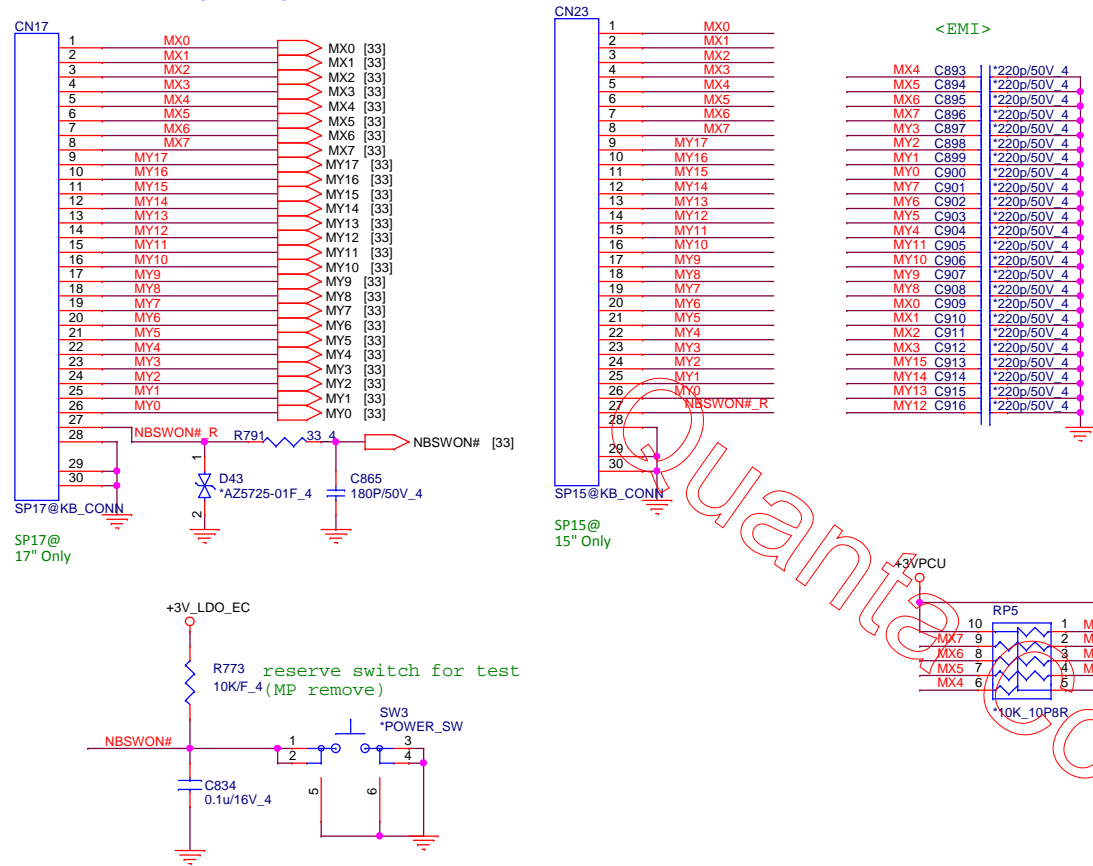
Layout set on BOT



 Quanta Computer Inc. PROJECT : ZAB	
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LED/HOLE/EMI	
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Rev 1A	



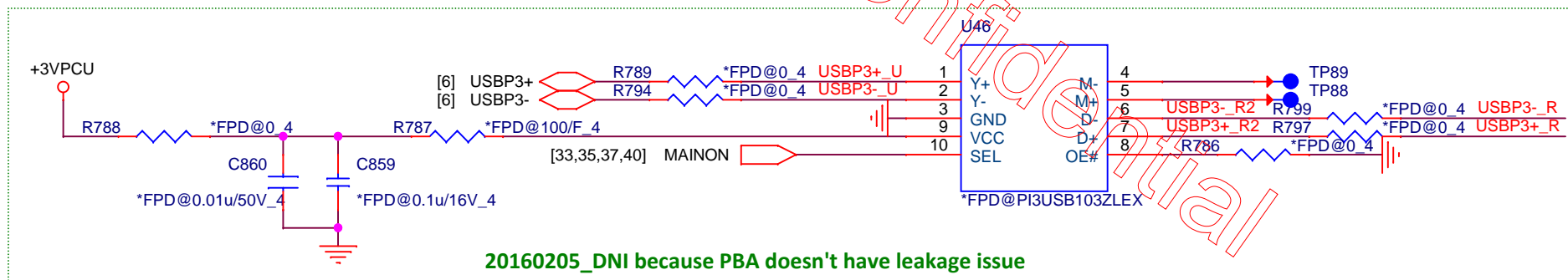
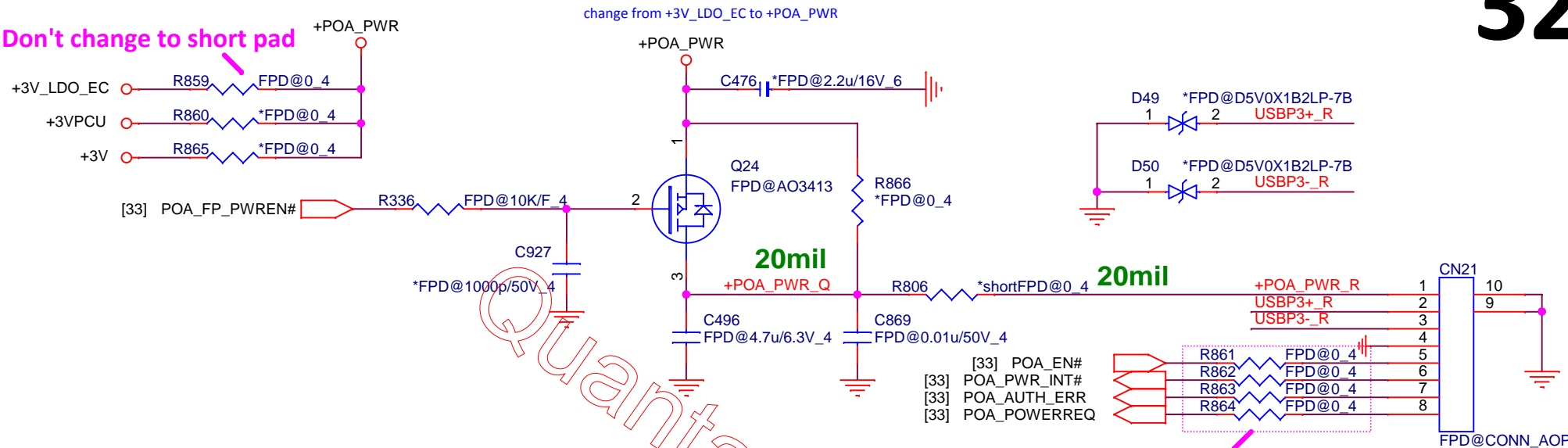
KEYBOARD (KBC)



POA(FPD) or PBA


32

Don't change to short pad



SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

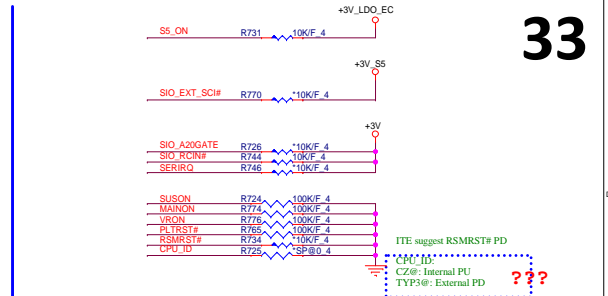
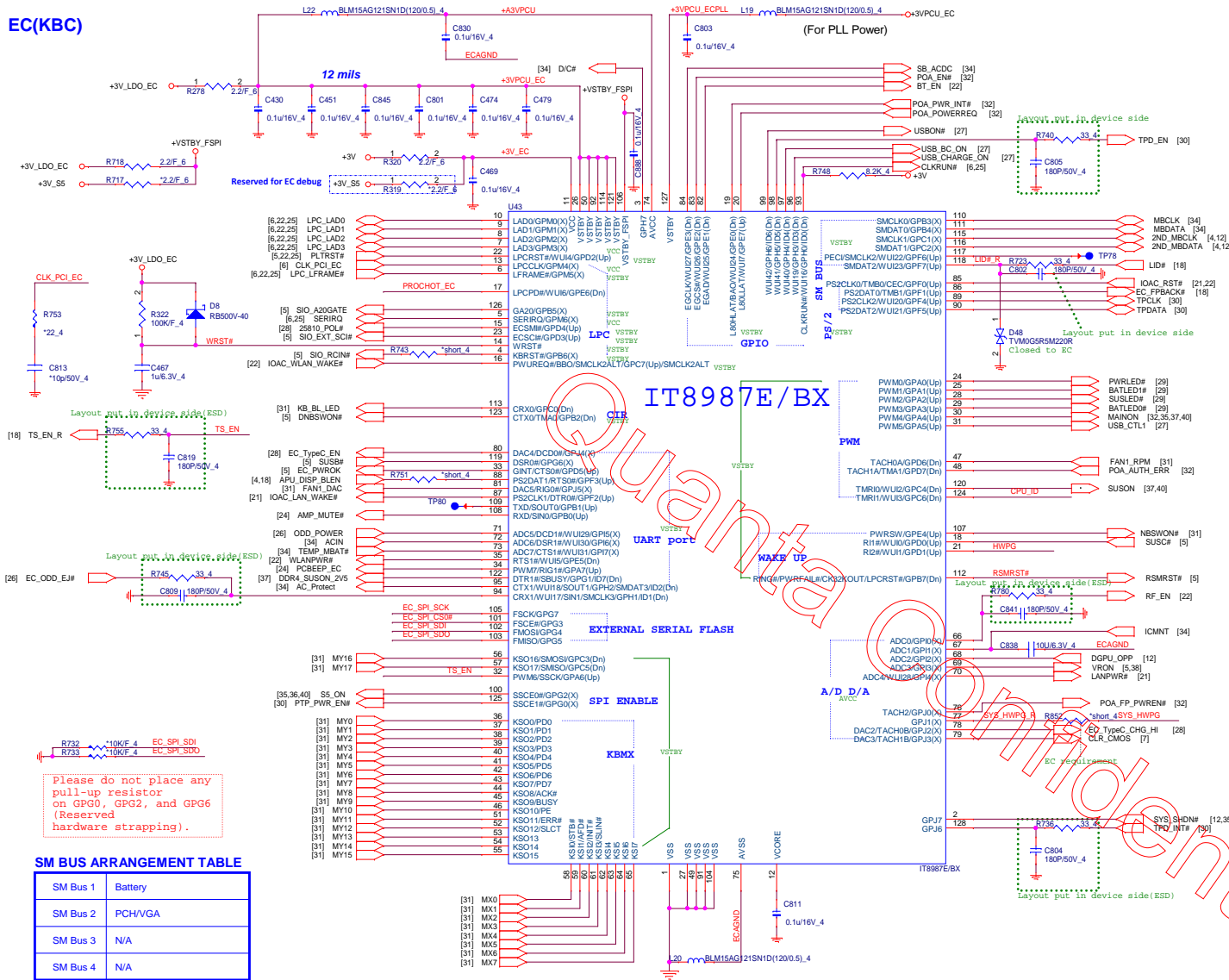
Spec define: High Active



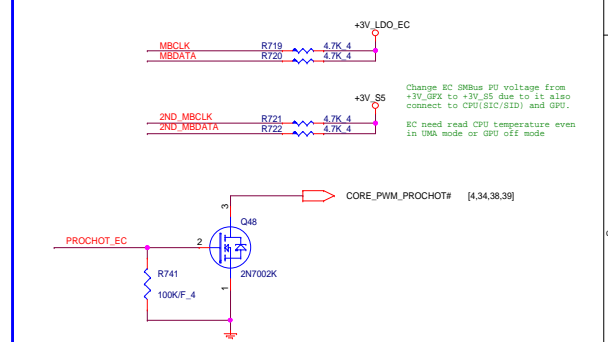
Quanta Computer Inc.

PROJECT : ZAB

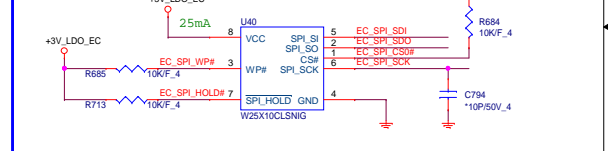
Size	Document Number	Rev
	POA	1A
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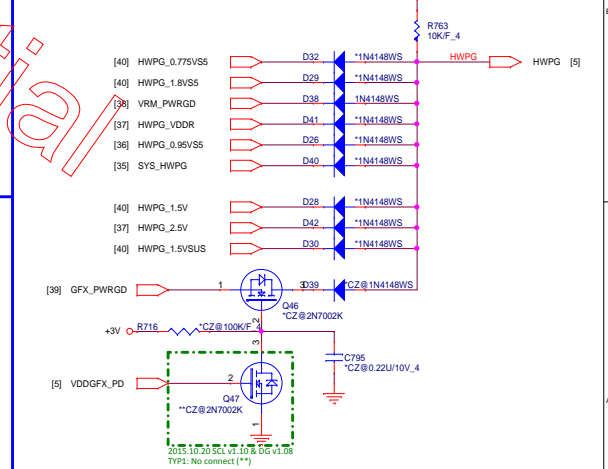
SM BUS PU(KBC)



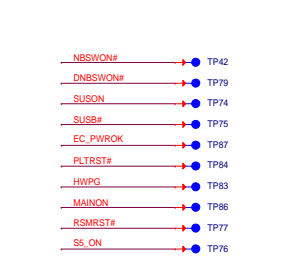
SPI NOR FLASH(128KB) (KBC)



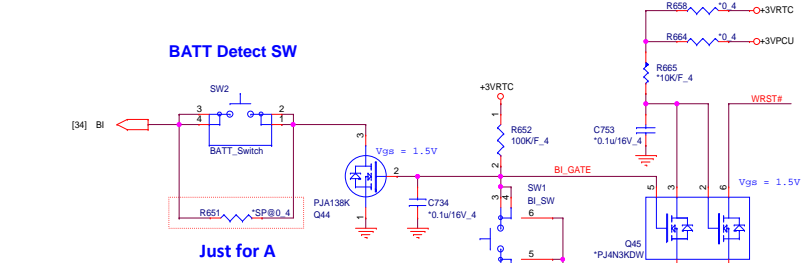
HWPG(KBC)



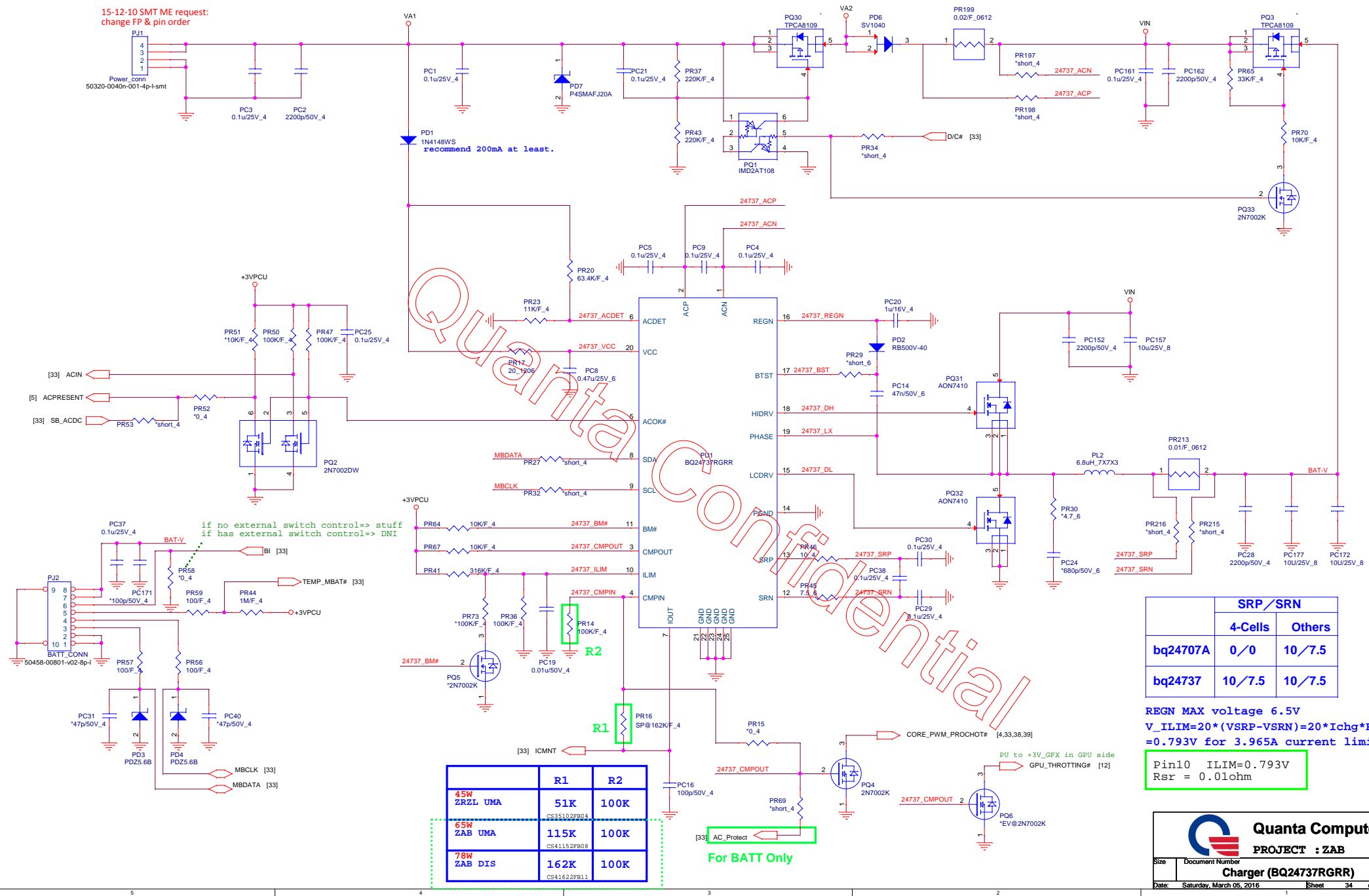
Power sequence



Battery B/I SW (SYP)



15-12-10 SMT ME request:
change FP & pin order



	SRP / SRN	
	4-Cells	Others
bq24707A	0 / 0	10 / 7.5
bq24737	10 / 7.5	10 / 7.5

REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr} = 0.793V$ for 3.965A current limit
 Pin10 ILIM=0.793V
 $R_{sr} = 0.01ohm$

	R1	R2
45W ZRZL UMA	51K CS35102PB04	100K
65W ZAB UMA	115K CS41152PB08	100K
78W ZAB DIS	162K CS41622PB11	100K

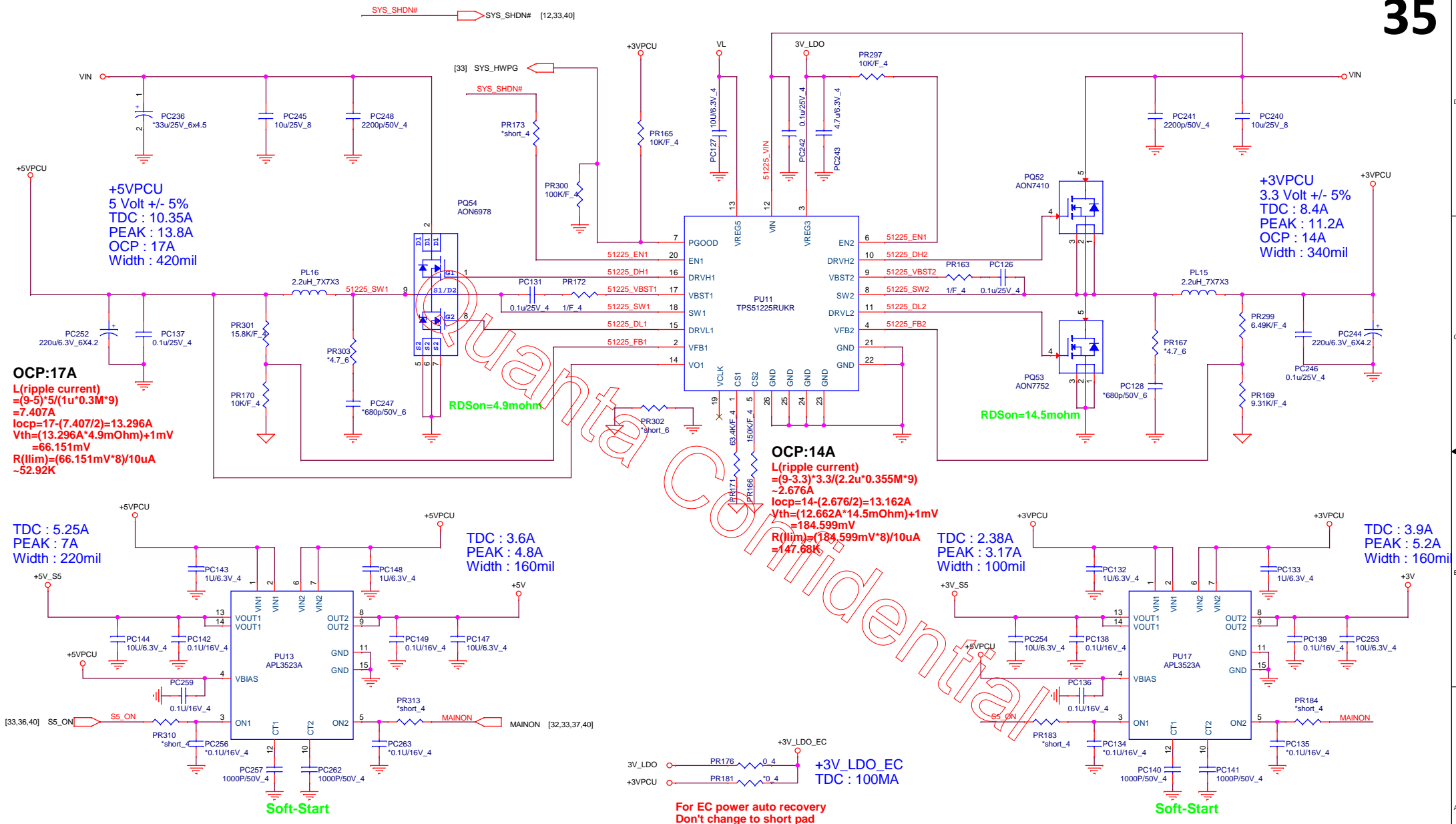
For BATT Only

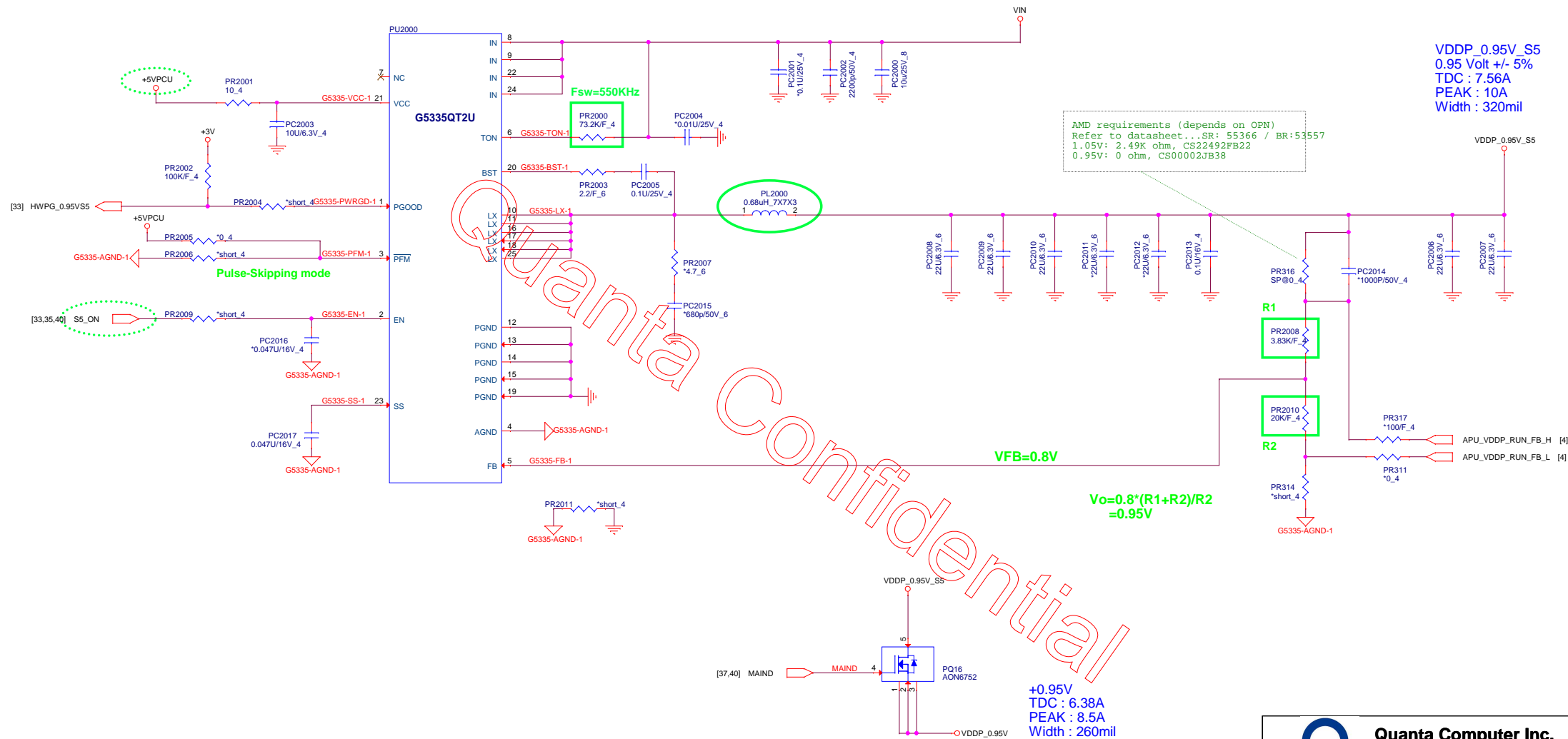
Quanta Computer Inc.
PROJECT : ZAB

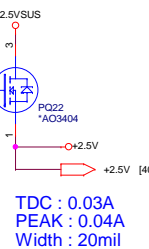
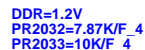
Size Document Number Rev 1A

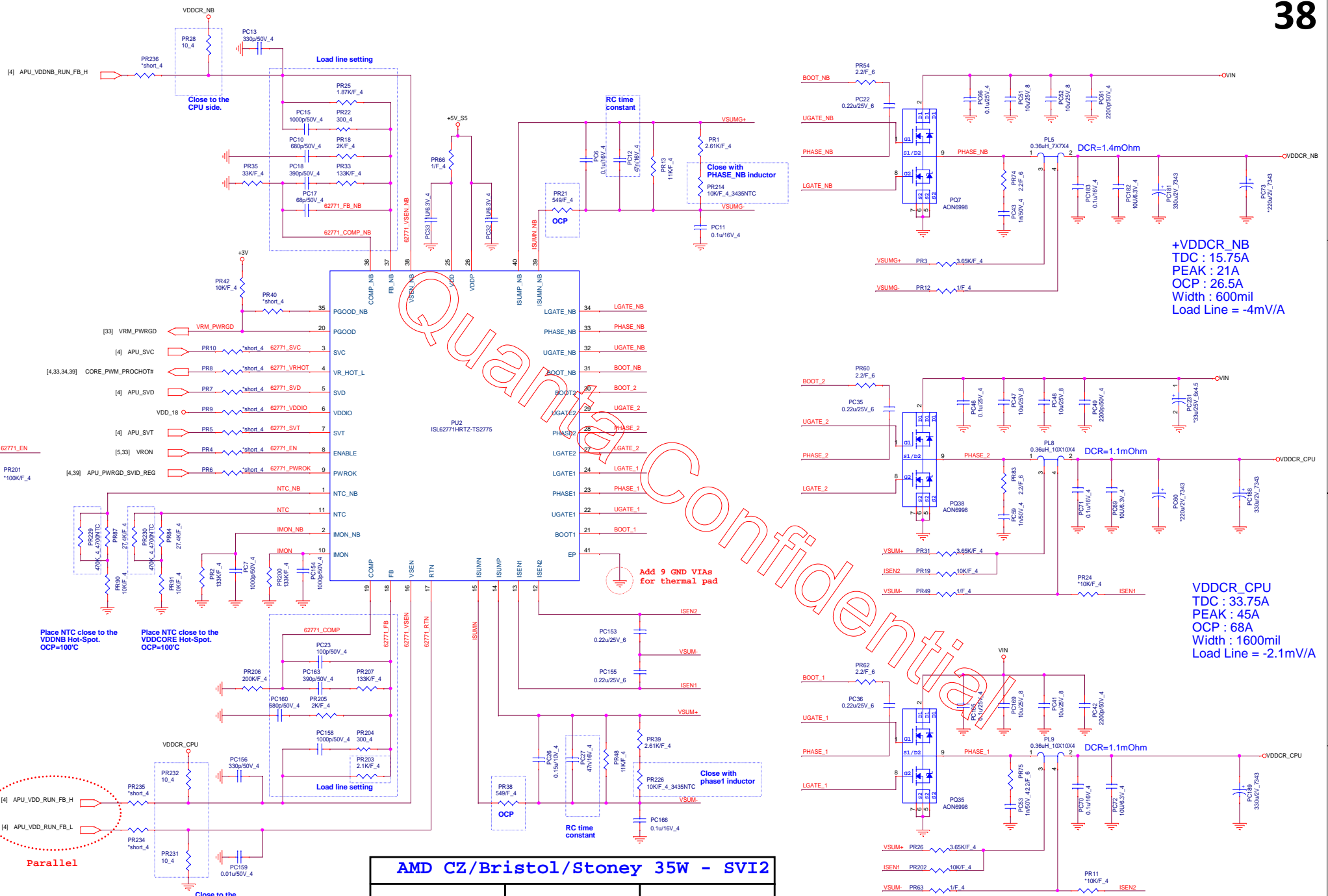
Charger (BQ24737RGR)

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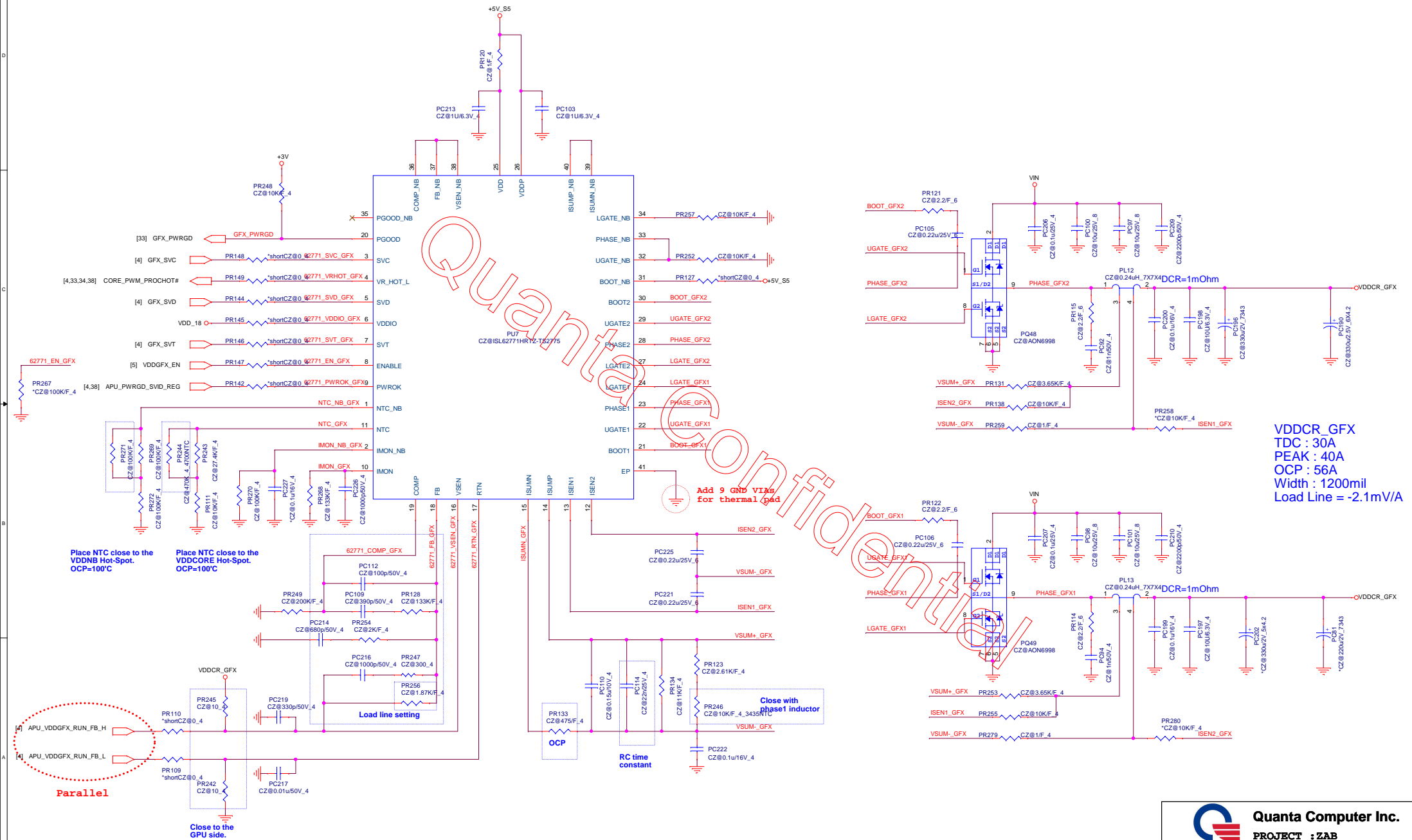


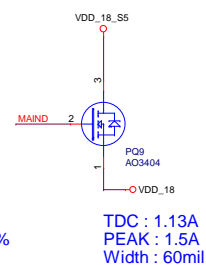
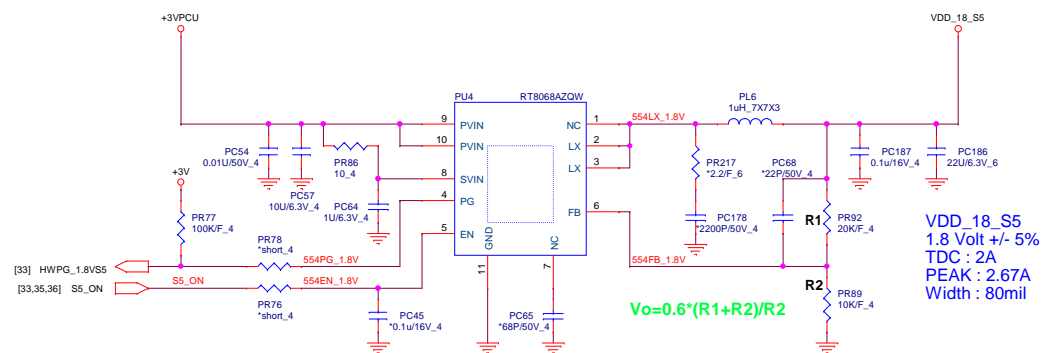




AMD CZ/Bristol/Stoney 35W - SVI2

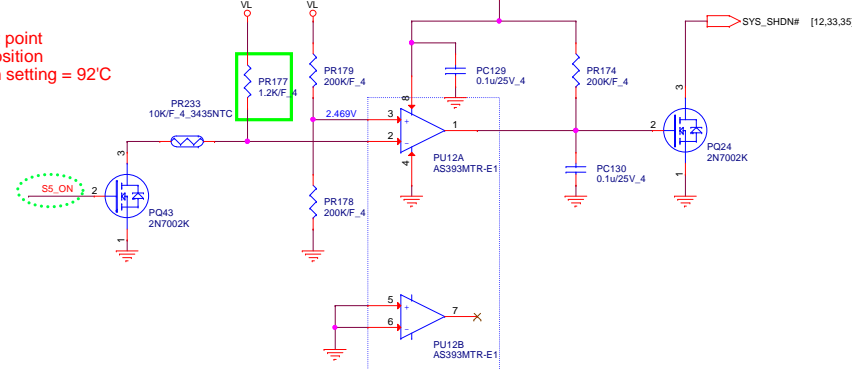
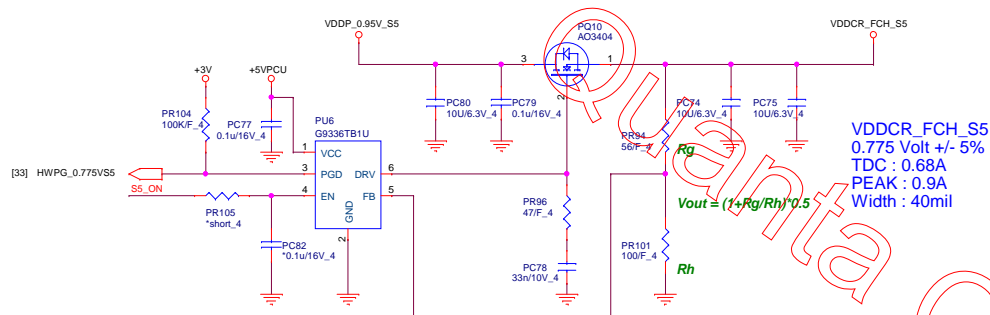
+VDDCR_NB TDC : 15.75A PEAK : 21A OCP : 26.5A Width : 600mil Load Line = -4mV/A	+VDDCR_CPU TDC : 33.75A PEAK : 45A OCP : 68A Width : 1600mil Load Line = -2.1mV/A	+VDDCR_GFX TDC : 30A PEAK : 40A OCP : 56A Width : 1200mil Load Line = -2.1mV/A
---	---	--



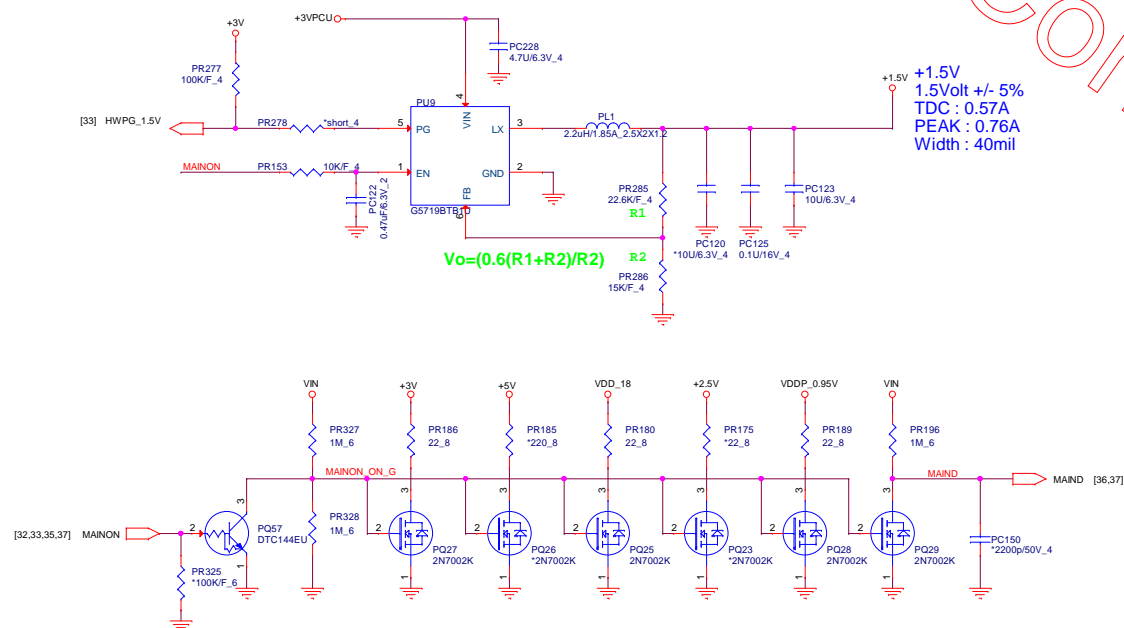
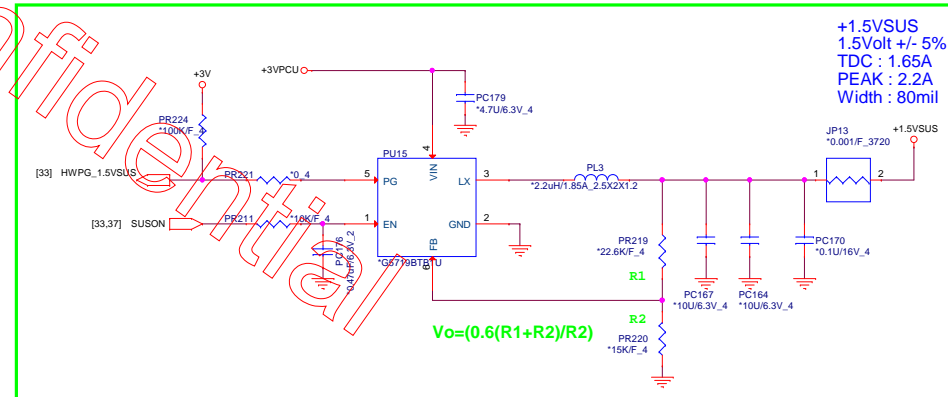


Thermal Protection

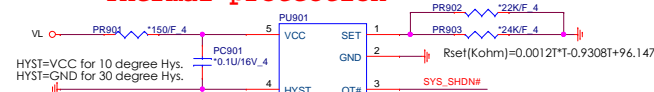
- (1) Need fine tune for thermal protect point
- (2) Note placement position
- (3) Thermal protection setting = 92°C



+1.5VSUS Reserve for +1.5V Wifi Card



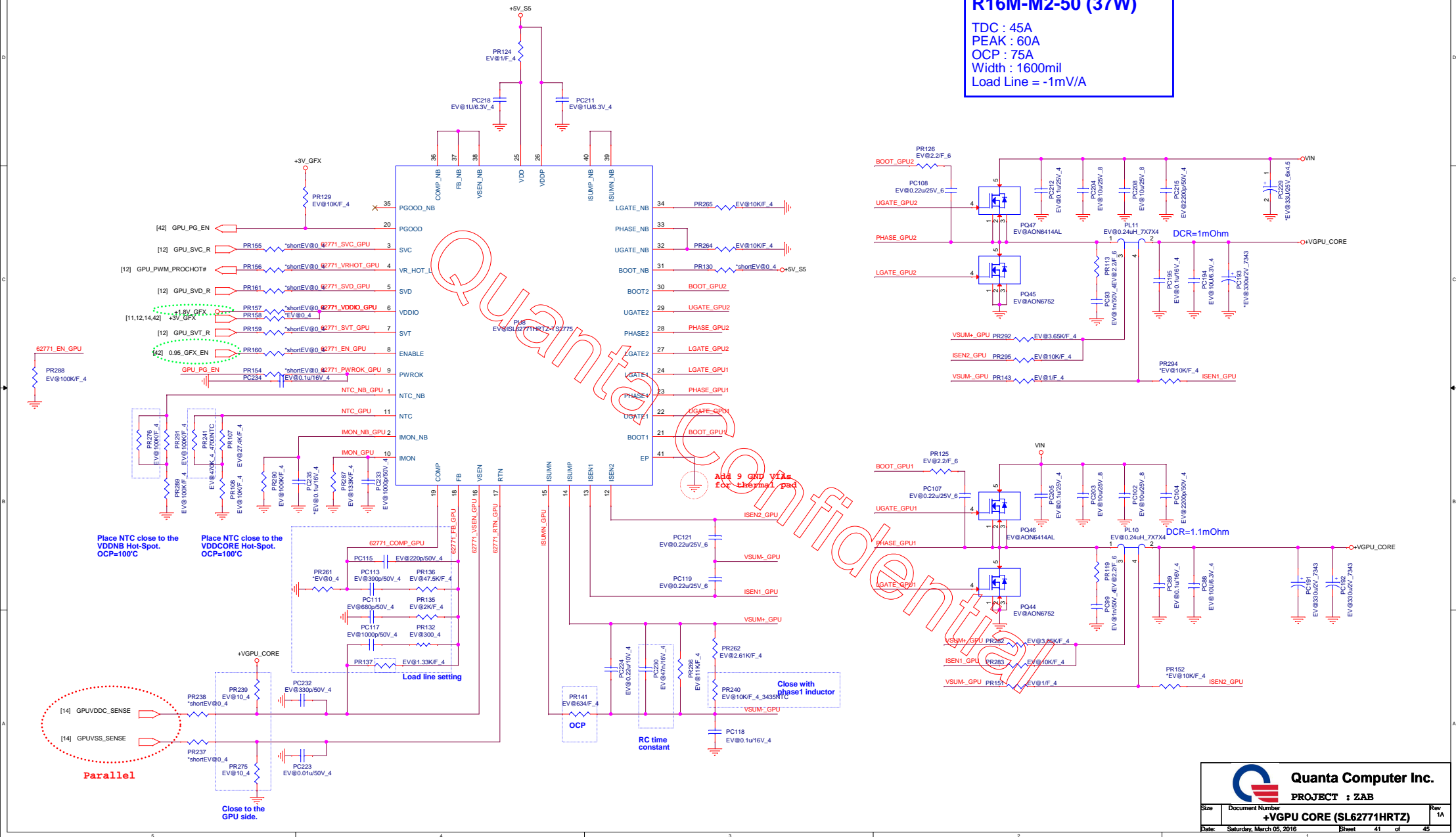
Thermal protection

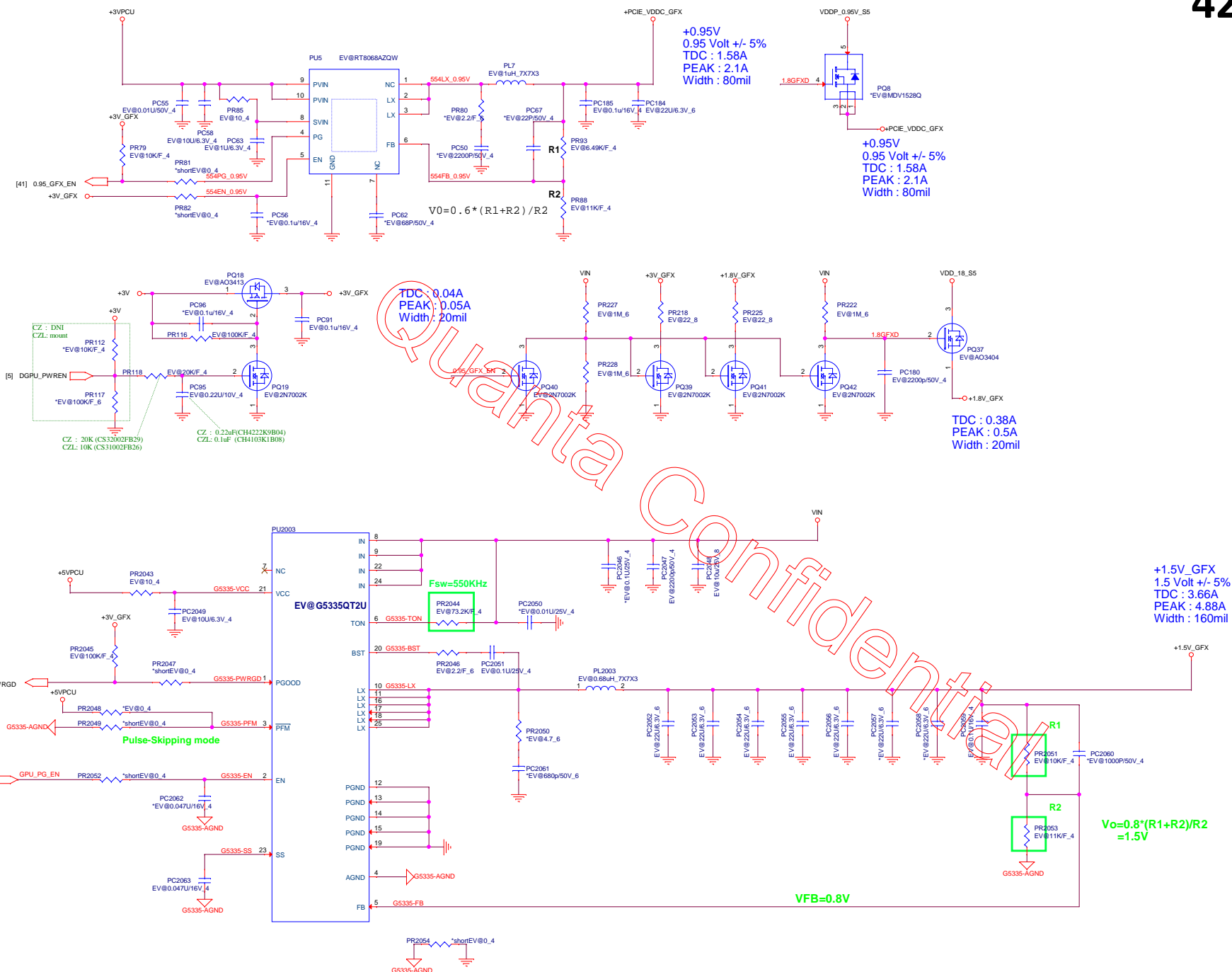


Interface SVI2

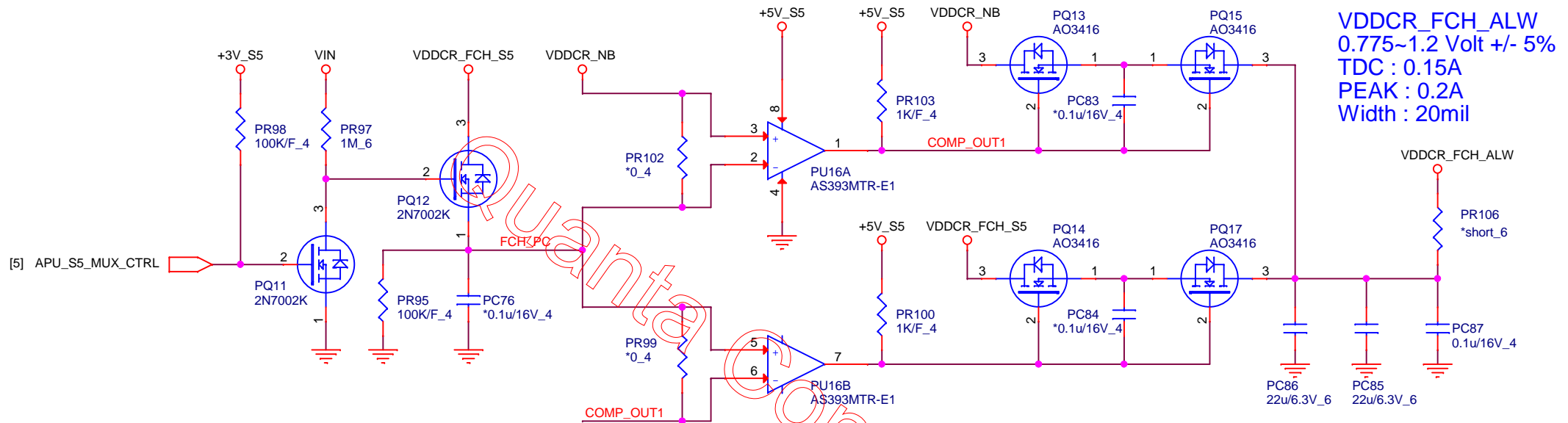
R16M-M2-50 (37W)

TDC : 45A
 PEAK : 60A
 OCP : 75A
 Width : 1600mil
 Load Line = -1mV/A





For Type 1 & 3



Quanta Computer Inc.

PROJECT : ZAB

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	VDDCR_FCH_ALW	1A
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Change List			Model	ZAB M/B	
MODEL	REV		Page	From	To
ZAB M/B	A	2015-11-03 Change DP to VGA IC from IT6516 to RTD2166 (cost) First Release	1		
			2		
			3		
			4		
			5		
			6		
			7		
			8		
			9		
			10		
			11		
			12		
			13		
			14		
			15		
			16		
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Power Rail	Description	Range	S0	S3	S5
VDDCR_CPU	APU power	0.75~1.5	ON	OFF	OFF
VDDCR_NB	APU NB power	0.75~1.2	ON	OFF	OFF
VDDCR_GFX	APU GFX power	0.75~1.2	ON	OFF	OFF
VDDCR_FCH_S5	APU FCH core logic power	0.775~1.2	ON	ON	ON
+SMDDR_VREF	DDR power	0.6	ON	ON	OFF
+SMDDR_VTT	DDR power	0.6	ON	OFF	OFF
+1.2VSUS	APU & DDR power	1.2	ON	ON	OFF
+2.5V	DDR power	2.5	ON	OFF	OFF
+1.5V	1.5V power rail	1.5	ON	OFF	OFF
+1.5VSUS	1.5V switched power rail	1.5	ON	ON	OFF
VDDP_0.95V	0.95V switched power rail	0.95	ON	OFF	OFF
VDDP_0.95V_S5	APU power	0.95	ON	ON	ON
VDD_18	1.8V switched power rail	1.8	ON	OFF	OFF
VDD_18_S5	1.8V power rail	1.8	ON	ON	ON
+3V	3.3V switched power rail	3.3	ON	OFF	OFF
+3V_S5	3.3V power rail	3.3	ON	ON	ON
+3VPCU	3.3V always	3.3	ON	ON	ON
+5V	5V switched power rail	5	ON	OFF	OFF
+5V_S5	5V power rail	5	ON	ON	ON
+5VPCU	5V always	5	ON	ON	ON
+VGPU_CORE	GPU power	0.8~1.225	ON	OFF	OFF
+1.5V_GFX	GPU power	1.5	ON	OFF	OFF
+PCIE_VDDC_GFX	GPU power	0.95	ON	OFF	OFF
+1.8V_GFX	GPU power	1.8	ON	OFF	OFF
+3V_GFX	GPU power	3.3	ON	OFF	OFF
VIN	Adaptor power supply	11.1~19	ON	ON	ON



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